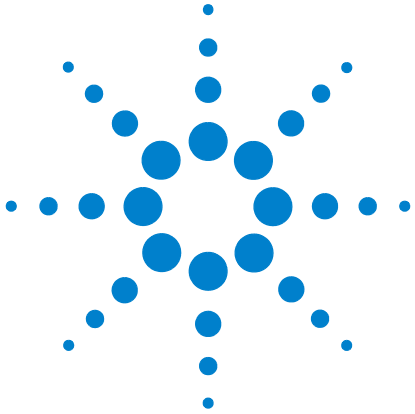

Agilent N5413A DDR2 Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

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DDR2 —Quick Reference

Table 1 DDR2 Cycles and Signals

NOTE: 1 = Single Ended signal; 2 = Differential signal; 3 = 2 x Single Ended signal

TEST	Cycle		Based on Test Definition						Required Connection Type to Perform Test on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)	√	√			√						√[1,2]				
tJIT(cc)	√	√			√						√[1,2]				
tERR(nper)	√	√			√						√[1,2]				
tCH(avg)	√	√			√						√[1,2]				
tCL(avg)	√	√			√						√[1,2]				
tJIT(duty)	√	√			√						√[1,2]				
tCK(avg)	√	√			√						√[1,2]				
VIH(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIH(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SlewR		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SlewF		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
AC Overshoot	√	√	√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
AC Undershoot	√	√	√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
VID(ac)		√		√	√				√[3]	√[3]	√[3]				
VIX(ac)		√		√	√				√[3]	√[3]	√[3]				
VOX(ac)	√			√					√[3]	√[3]					
tAC	√		√		√				√[1]	√[1,2]	√[1,2]				√
tDQSCK	√			√	√				√[1]	√[1,2]	√[1,2]				√
tHZ(DQ)	√		√		√				√[1]	√[1,2]	√[1,2]				√
tLZ(DQS)	√			√	√				√[1]	√[1,2]	√[1,2]				√
tLZ(DQ)	√		√		√				√[1]	√[1,2]	√[1,2]				√

Table 1 DDR2 Cycles and Signals

NOTE: 1 = Single Ended signal; 2 = Differential signal; 3 = 2 x Single Ended signal

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tDQSQ	√		√						√[1]	√[1,2]					√
tQH	√		√						√[1]	√[1,2]					√
tDQSS		√		√	√				√[1]	√[1,2]	√[1,2]				√
tDQSH		√		√					√[1]	√[1,2]					√
tDQSL		√		√					√[1]	√[1,2]					√
tDSS		√		√	√				√[1]	√[1,2]	√[1,2]				√
tDSH		√		√	√				√[1]	√[1,2]	√[1,2]				√
tWPST		√		√					√[1]	√[1,2]					√
tWPRE		√		√					√[1]	√[1,2]					√
tRPRE	√			√					√[1]	√[1,2]					√
tRPST	√			√					√[1]	√[1,2]					√
tDS(base)		√	√					√	√[1]	√[2]				√[1]	√
tDH(base)		√	√					√	√[1]	√[2]				√[1]	√
tDS1(base)		√	√					√	√[1]	√[1]				√[1]	√
tDH1(base)		√	√					√	√[1]	√[1]				√[1]	√
tIS(base)		√			√	√	√				√[1,2]	√[1]	√[1]		√
tIH(base)		√			√	√	√				√[1,2]	√[1]	√[1]		√
Eye Diagram - Read	√		√	√					√[1]	√[1,2]					
Eye Diagram - Write		√	√	√					√[1]	√[1,2]					

DDR2 Compliance Test Application — At A Glance

The Agilent N5413A DDR2 Compliance Test Application is a DDR2 (Double Data Rate 2) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications. The software helps you in testing all the un-buffered DDR2 device under test (DUT) compliance, with the Agilent 80000B or 90000A Series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR2 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Custom Mode Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform non-JEDEC specific speed signal testing.

The DDR2 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Allows you to customize the test limits in the application which determines the pass or/and fail of each test.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Custom Mode tests - 3 probes.

NOTE The tests performed by the DDR2 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

DDR2 SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79-2E* and *JESD208* document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR2 automated tests, you need the following equipment and software:

- 80000B, 9000A, or 90000A Series Infiniium Digital Storage Oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Version 5.71 or greater of the Infiniium software (80000B series Infiniium Digital Storage Oscilloscope) OR
- Version 2.01 or greater of the Infiniium software (90000A series Infiniium Digital Storage Oscilloscope OR 9000A series Infiniium Oscilloscope).
- N5413A DDR2 Compliance Test Application, version 2.41 and higher.
- RAM reliability test software.
- 1169A, 1168A, 1134A, 1132A or 1131A InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head with N5426A or N5451A ZIF tip accessories.
- Any computer motherboard system that supports DDR2 memory.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- N5413A DDR2 Compliance Test Application license.
- N5414A InfiniiScan software license.
- E2688A Serial Data Analysis and Clock Recovery software license.
- N5404A Deep memory option (optional).

In This Book

This manual describes the tests that are performed by the DDR2 Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79-2E* and *JESD208,* and it describes how the tests are performed.

- Chapter 1, “Installing the DDR2 Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DDR2 Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Measurement Clock Tests” describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.
- Chapter 4, “Single-Ended Signals AC Input Parameters Tests” shows how to run the single-ended signals AC input parameters tests. This chapter includes input signal maximum peak to peak swing tests, input signal minimum slew rate (rising) tests, input signal minimum slew rate (falling) tests, input logic HIGH tests and input logic LOW tests.
- Chapter 5, “Single-Ended Signals Overshoot/Undershoot Tests” describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 6, “Differential Signals AC Input Parameters Tests” describes the V_{ID} AC differential input voltage tests and V_{IX} AC differential cross point voltage tests.
- Chapter 7, “Differential Signal AC Output Parameters Tests” contains more information on the V_{OX} AC differential cross point voltage tests.
- Chapter 8, “Clock Timing (CT) Tests” describes the clock timing operating conditions of DDR2 SDRAM as defined in the specification.
- Chapter 9, “Data Strobe Timing (DST) Tests” describes various data strobe timing tests including tHZ(DQ), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE and tRPST tests.
- Chapter 10, “Data Timing Tests” describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.
- Chapter 11, “Command and Address Timing (CAT) Tests” describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.

- Chapter 12, “Custom Mode Read-Write Eye-Diagram Tests” describes the user defined real-time eye-diagram test for read cycle and write cycle.
- Chapter 13, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the DDR2 automated tests.
- Chapter 14, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for DDR2 testing.

See Also

The DDR2 Compliance Test Application’s online help, which describes:

- Starting the DDR2 compliance test application.
  - To view/minimize the task flow pane
  - To view/hide the toolbar
- Creating or Opening a Test Project
- Setting up DDR2 test environment.
- Selecting tests.
- Configuring tests.
- User-Defined compliance limits.
- Connecting the oscilloscope to the DUT.
- Running tests.
- Viewing test results.
  - To delete trials from the results
  - To show reference images and flash mask hits
  - To change the display settings
  - To change the remote settings
  - To change the margin thresholds and trial report display
  - To change the user prompt option
- To change the auto-recovery option
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

Contact Agilent

For more information on DDR2 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

Taiwan:

(tel) 0800 047 866

(fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100

(fax) (65) 6755 0042

E-mail: tm_ap@agilent.com

Contents

10 Data Timing Tests

11 Command and Address Timing (CAT) Tests

1 Installing the DDR2 Compliance Test Application

If you purchased the N5413A DDR2 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version 1.31 or greater of the Infiniium software (90000A series Infiniium Digital Storage Oscilloscope) OR version 5.60 or greater of the Infiniium software (80000B series Infiniium Digital Storage Oscilloscope), by choosing Help>About Infiniium... from the main menu.

2 To obtain the DDR2 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/N5413A.

3 The link for DDR2 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the DDR2 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR2 application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR2 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 13, "Calibrating the Infiniium Oscilloscope and Probe".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR2 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR2 memory.

2 To start the DDR2 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DDR2 Test**.

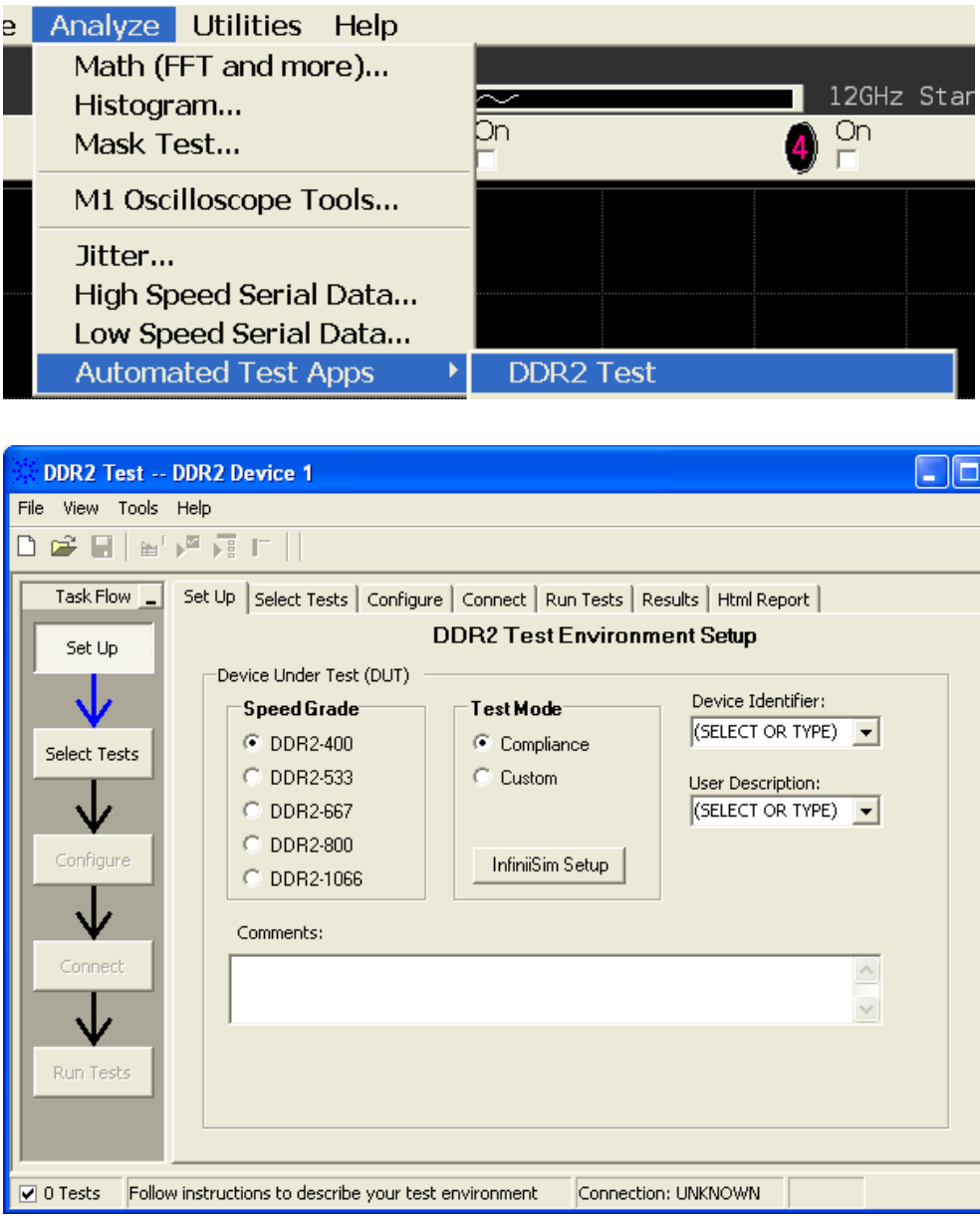

Figure 1 The DDR2 Compliance Test Application

NOTE If DDR2 Test does not appear in the Automated Test Apps menu, the DDR2 Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR2 Compliance Test Application").

Figure 1 shows the DDR2 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DDR2 application, each channel's probe is configured as single-ended or differential depending on the last DDR2 test that was run.

Online Help Topics

For information on using the DDR2 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The DDR2 Compliance Test Application's online help describes:

- Starting the DDR2 compliance test application.
  - To view/minimize the task flow pane
  - To view/hide the toolbar
- Creating or Opening a Test Project
- Setting up DDR2 test environment.
- Selecting tests.
- Configuring tests.
- User-Defined compliance limits.
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  - To delete trials from the results
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  - To change the display settings
  - To change the remote settings
  - To change the margin thresholds and trial report display
  - To change the user prompt option
- To change the auto-recovery option
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

3 Measurement Clock Tests

This section provides the Methods of Implementation (MOIs) for Rising Edge and Pulse Measurements Clock tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Measurement Clock Tests

When performing the Measurement Clock tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connections for Rising Edge and Pulse Measurement Clock tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

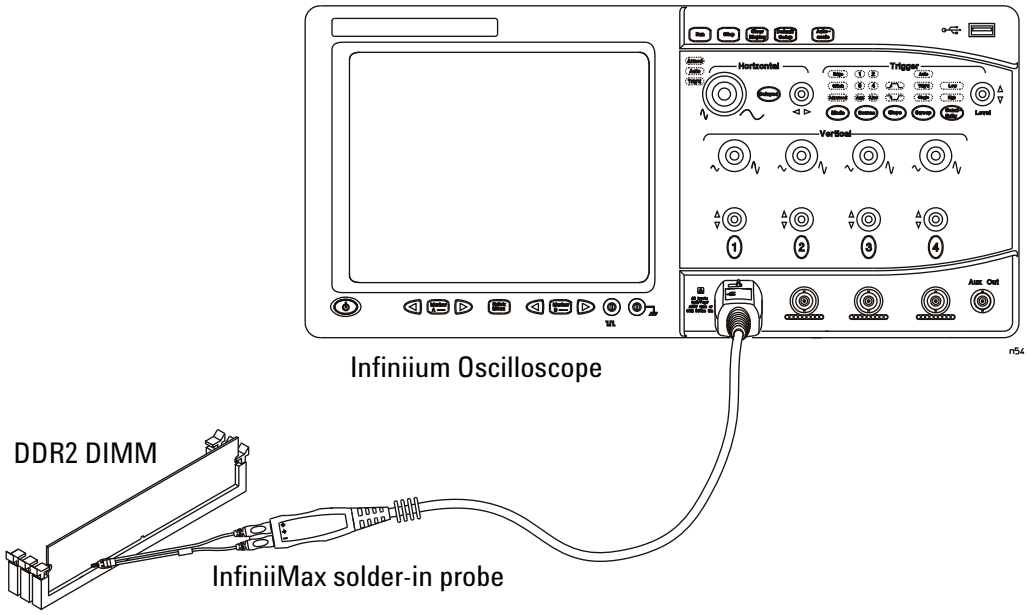

Figure 2 Probing for Measurement Clock Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channel shown in Figure 2 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system

by producing a repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUT on the DDR2 devices.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For the DDR2 Measurement Clock tests, you can select either DDR2-667, DDR2-800 and DDR2-1066 speed grade. If other Speed Grade is selected, the Measurement Clock test options will not be displayed at the Select tab.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

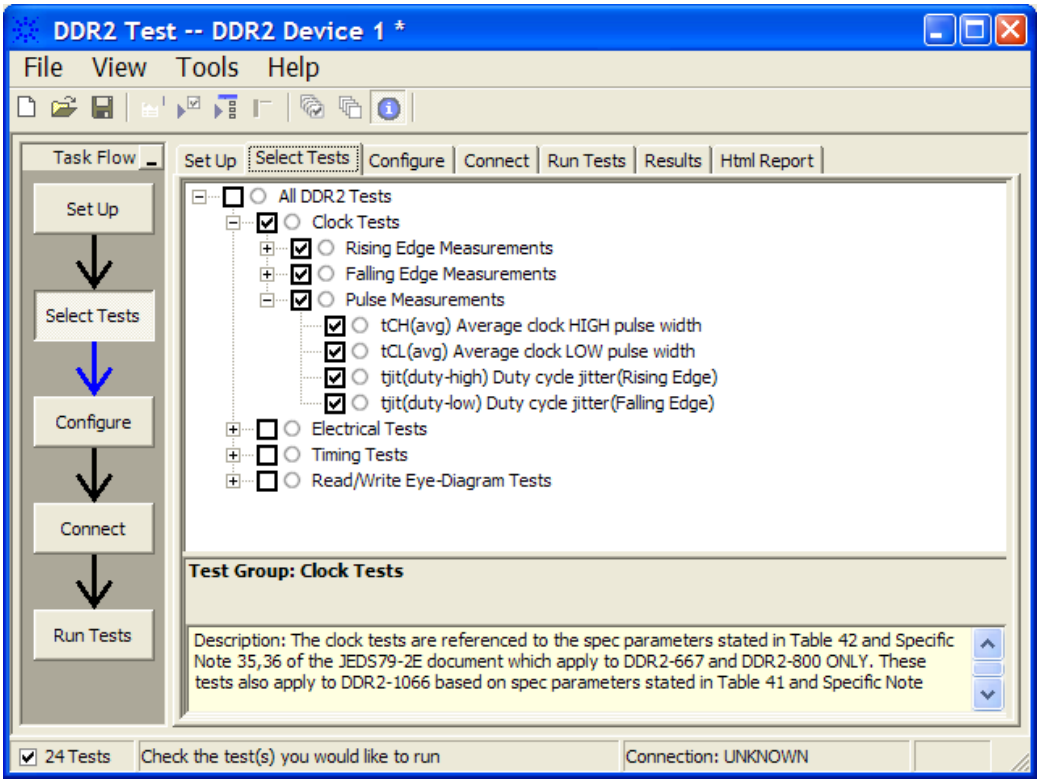

Figure 3 Selecting Measurement Clock Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the test, and view the test results.

Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement and Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. You can specify the rising and/or the falling edge of your signal for this measurement.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 2 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-125	125	-100	100	ps	35

Table 3 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Clock Period Jitter	tJIT(per)	-90	90	ps	30

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E* and Specific Note 30 in the *JESD208*.

Pass Condition

The tJIT(per) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.

2 Compare periods with the new average.

3 Check the results for the smallest and largest values (worst case

4 values).

5 Compare the test results against the compliance test limits.

Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as Falling Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge. The tJIT(cc) Falling Edge Measurement measures the clock period from the falling edge to falling edge. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 4 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	-250	250	-200	200	ps	35

Table 5 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	-180	180	ps	30

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E* and Specific Note 30 in the *JESD208*.

Pass Condition

The tJIT(cc) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the difference between every adjacent pair of periods.
2. Generate 201 measurement results.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Cumulative Error - tERR(n per) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of "n" (for "n" cycle) where n>5 but less than 50.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 6 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6....10, inclusive	tERR(6-10 per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11...50, inclusive	tERR(11-50 per)	-450	450	-450	450	ps	35

Table 7 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		min	max		
Cumulative error across 2 cycles	tERR(2per)	-132	132	ps	30
Cumulative error across 3 cycles	tERR(3per)	-157	157	ps	30
Cumulative error across 4 cycles	tERR(4per)	-175	175	ps	30
Cumulative error across 5 cycles	tERR(5per)	-188	188	ps	30
Cumulative error across n cycles, n = 6....10, inclusive	tERR(6-10 per)	-250	250	ps	30
Cumulative error across n cycles, n = 11...50, inclusive	tERR(11-50 per)	-425	425	ps	30

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E* and Specific Note 30 in the *JESD208*.

Pass Condition

The tERR measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. Check the results for the smallest and largest values (worst case values).
3. Compare the results against the compliance test limits.
4. tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods and tERR(5per) uses 5 periods.
5. tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.
6. tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Average HIGH Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 8 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36

Table 9 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	tCK(avg)	30,31

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E* and Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 10 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36

Table 11 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Average clock LOW pulse width	tCL(avg)	0.48	0.52	tCK(avg)	30,31

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E* and Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare results against the compliance test limits.

Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average HIGH and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average HIGH Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 12 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	ps	35

Table 13 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Duty cycle jitter	tJIT(duty)	-75	75	ps	30

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E* and Specific Note 30 in the *JESD208*.

Pass Condition

The tJIT(duty) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH)

1 This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.

2 Measure the difference between high pulse width, and the average. Save the answer as the measurement result.

3 Compare the high pulse width with the new average.

4 Check the results for the smallest and largest values (worst case values).

5 Compare the test results against the compliance test limits.

tJIT(LH)

1 This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses LOW pulse widths for testing comparison.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(avg) Falling Edge Measurements measures from the falling edge to the falling edge.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 14 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	35,36

Test Definition Notes from the Specification

Table 15 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Average clock period	tCK(avg)	1875	7500	ps	30,31

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E* and Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding “window” of 200 cycles.
2. Calculate the average period value for periods 1-200, 2-201 and 3-202.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

4 Single-Ended Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

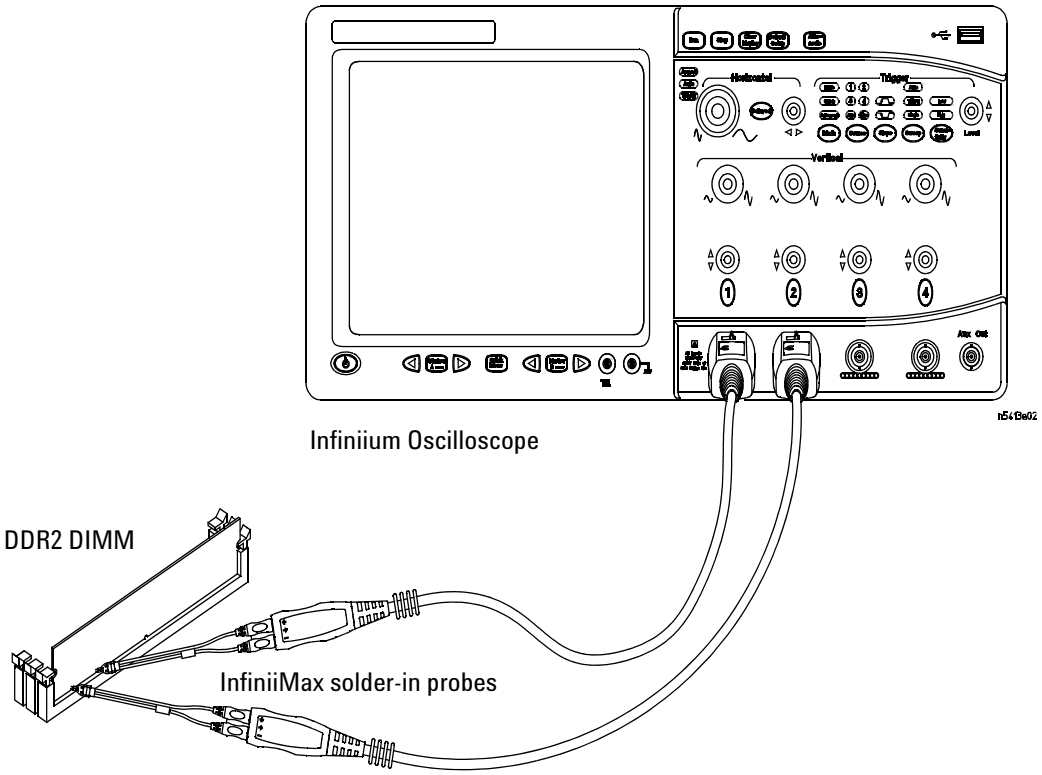

Figure 4 Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 4 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

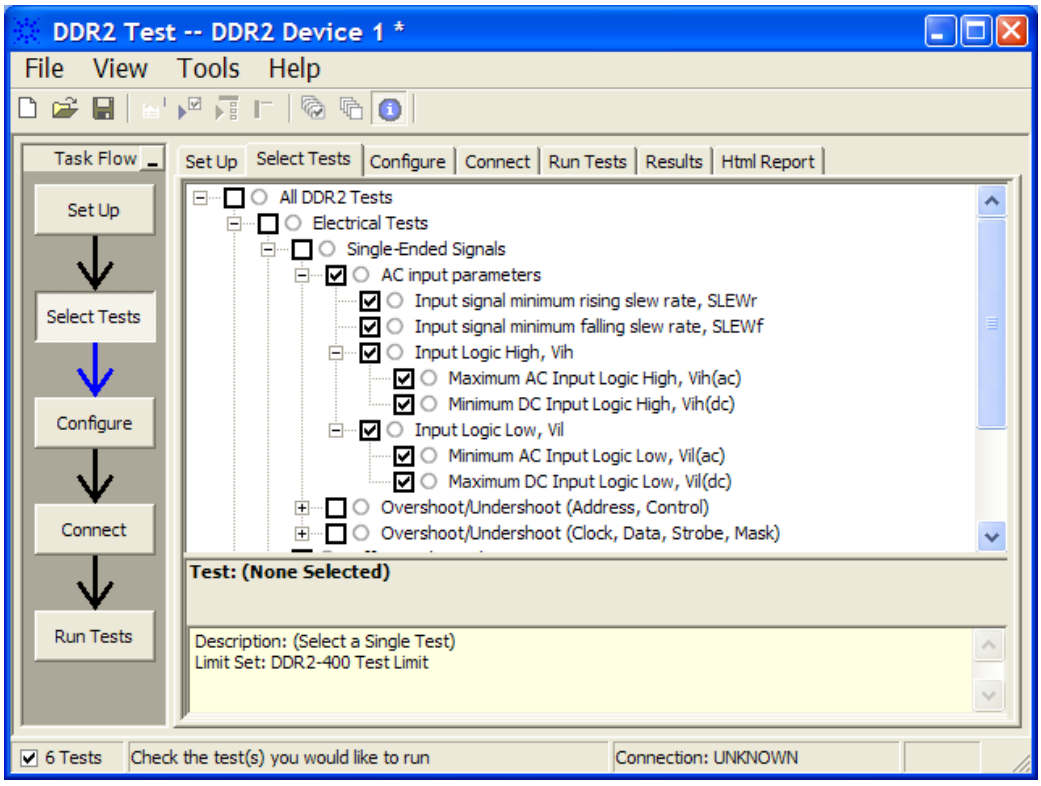

Figure 5 Selecting Single-Ended Signals AC Input Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{IH(AC)}$ Test Method of Implementation

V_{IH} Input Logic HIGH test can be divided into two sub tests: $V_{IH(AC)}$ test and $V_{IH(DC)}$ test.

$V_{IH(AC)}$ - Maximum AC Input Logic HIGH.

For PUT is DQ or DM: The purpose of this test is to verify that voltage level of test signal at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint is greater than the conformance lower limits of the VIH(AC) value specified in the JEDEC specification.

For PUT other than DQ or DM: The purpose of this test is to verify that the mode of histogram of the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ, DM, or DQS

Test Definition Notes from the Specification

Table 16 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IH(AC)}$	ac input logic HIGH	V_{REF} + 0.250	$V_{DDQ}+V_{PEAK}$	V_{REF} + 0.200	$V_{DDQ}+V_{PEAK}$	V	1

Table 17 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IH(AC)}$	ac input logic HIGH	V_{REF} + 0.200	-	V	-

Test References

See Table 20 - Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

For PUT is DQ or DM: The voltage level at at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint for the high level voltage shall be greater than or equal to the minimum VIH (AC) value.

For PUT other than DQ or DM: The mode value of the high level voltage should be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

For PUT is DQ or DM:

1. Pre-condition the oscilloscope setting.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use the Setup time and Hold time to find and capture the Write cycle.
4. Find the DQS midpoint and the value of tDS (DM and DQ input setup time in JEDEC specification) which is due to the speed grade.
5. Calculate the time where the test result is taken. Calculation is expressed as: $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
6. Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IH(AC)}$.

7 When multiple trials are performed, the smallest value (worst case) among all the trials are used as the test result for $V_{IH(AC)}$.

8 Compare the test result against the compliance test limit.

For PUT other than DQ or DM:

1 Pre-condition the oscilloscope setting.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use the Setup time and Hold time to find and capture the Write cycle.

4 Check for the same consecutive logic bits to determine the valid sampling window.

5 Setup the histogram function settings. Use the histogram 'Mode' value as the test result for $V_{IH(AC)}$.

6 When multiple trials are performed, the smallest value (worst case) among all the trials are used as the test result for $V_{IH(AC)}$.

7 Compare the test result against the compliance test limit.

$V_{IH(DC)}$ Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic HIGH.

For PUT is DQ or DM: The purpose of this test is to verify that the min of histogram of the high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

For PUT other than DQ or DM: The purpose of this test is to verify that the mode of histogram of the high level voltage value of the test signal within a valid sampling window is within the conformance limits of the VIH(DC) value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ, DM, or DQS

Test Definition Notes from the Specification

Table 18 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	dc input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Table 19 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	dc input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

For PUT is DQ or DM: The minimum value of test signal from tDS before DQS midpoint to tDH after DQS midpoint for the high level voltage shall be greater than or equal to the minimum VIH (DC) value.

For PUT other than DQ or DM: The mode value for the high level voltage shall be greater than or equal to the minimum $V_{IH(DC)}$ value.

Measurement Algorithm

For PUT is DQ or DM:

1 Pre-condition the oscilloscope setting.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use the Setup time and Hold time to find and capture the Write cycle.

4 Setup the histogram function settings where the X region is:

- Ax: X-time position where tDS(DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint. *Mathematically, $Ax=T_{DQS\ Midpoint} - tDS$.
- Bx: X-time position where tDH(DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint. *Mathematically, $Bx=T_{DQS\ Midpoint} + tDH$.

Use the histogram 'Min' value as the test result for $V_{IH(DC)}$.

5 When multiple trials are performed, the smallest value (worst case) among all the trials are used as the test result for $V_{IH(DC)}$.

6 Compare the test result against the compliance test limit.

For PUT other than DQ or DM:

1 Pre-condition the oscilloscope setting.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use the Setup time and Hold time to find and capture the Write cycle.

4 Check for the same consecutive logic bits to determine the valid sampling window.

5 Setup the histogram function settings. Use the histogram 'Mode' value as the test result for $V_{IH(DC)}$.

6 When multiple trials are performed, the smallest value (worst case) among all the trials are used as the test result for $V_{IH(DC)}$.

7 Compare the test result against the compliance test limit.

$V_{IL(AC)}$ Test Method of Implementation

V_{IL} AC Input Logic Low test can be divided into two sub tests: $V_{IL(AC)}$ test and $V_{IL(DC)}$ test.

$V_{IL(AC)}$ - Minimum AC Input Logic Low.

For PUT is DQ or DM: The purpose of this test is to verify that voltage level of test signal at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint is lower than the conformance maximum limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

For PUT other than DQ or DM: The purpose of this test is to verify that the mode of the low level voltage value of the histogram for the test signal is lower than the conformance maximum limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

The value of V_{SSQ} which directly affect the conformance upper limit is set to 0V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{SSQ}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ, DM, or DQS

Test Definition Notes from the Specification

Table 20 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IL(AC)}$	ac input logic LOW	V_{SSQ}-V_{PEAK}	V_{REF} - 0.250	V_{SSQ}-V_{PEAK}	V_{REF} - 0.200	V	1

Table 21 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IL(AC)}$	ac input logic LOW	-	V_{REF} - 0.200	V	-

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

For PUT is DQ or DM: The voltage level at at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{IL(AC)}$ value.

For PUT other than DQ or DM: The mode value of the low level voltage should be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

For PUT is DQ or DM:

1. Pre-condition the oscilloscope setting.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use the Setup time and Hold time to find and capture the Write cycle.
4. Find the DQS midpoint and the value of tDS (DM and DQ input setup time in JEDEC specification) which is due to the speed grade.

5 Calculate the time where the test result is taken. Calculation is expressed as: $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.

6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IL(AC)}$.

7 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{IL(AC)}$.

8 Compare the test result against the compliance test limit.

For PUT other than DQ or DM:

1 Pre-condition the oscilloscope setting.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use the Setup time and Hold time to find and capture the Write cycle.

4 Check for the same consecutive logic bits to determine the valid sampling window.

5 Setup the histogram function settings. Use histogram 'Mode' value as the test result for $V_{IL(AC)}$.

6 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{IL(AC)}$.

7 Compare the test result against the compliance test limit.

$V_{IL(DC)}$ Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low.

For PUT is DQ or DM: The purpose of this test is to verify that the max of histogram of the low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

For PUT other than DQ or DM: The purpose of this test is to verify that the mode of the histogram of the low level voltage value of the test signal within a valid sampling window is within the conformance maximum limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ, DM, or DQS

Test Definition Notes from the Specification

Table 22 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	dc input logic LOW	-0.3	V_{REF} - 0.125	V	-

Table 23 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	dc input logic LOW	-0.3	V_{REF} - 0.125	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

For PUT is DQ or DM: The maximum value of test signal from tDS before DQS midpoint to tDH after DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{IL(DC)}$ value.

For PUT other than DQ or DM: The mode value for the histogram of the low level voltage should be less than or equal to the maximum $V_{IL(DC)}$ value.

Measurement Algorithm

For PUT is DQ or DM:

1. Pre-condition the oscilloscope setting.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use the Setup time and Hold time to find and capture the Write cycle.
4. Setup the histogram function settings where the X region is:
   - Ax: X-time position where tDS(DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint. *Mathematically, $Ax=T_{DQS\ Midpoint} - tDS$.
   - Bx: X-time position where tDH(DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint. *Mathematically, $Bx=T_{DQS\ Midpoint} + tDH$.

   Use the histogram 'Max' value as the test result for $V_{IL(DC)}$.

5 When multiple trials are performed, the largest value (worst case) among all the trials are used as the test result for $V_{IL(DC)}$.

6 Compare the test result against the compliance test limit.

For PUT other than DQ or DM:

1 Pre-condition the oscilloscope setting.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use the Setup time and Hold time to find and capture the Write cycle.

4 Check for the same consecutive logic bits to determine the valid sampling window.

5 Setup the histogram function settings. Use the histogram 'Mode' value as the test result for $V_{IL(DC)}$.

6 When multiple trials are performed, the largest value (worst case) among all the trials are used as the test result for $V_{IL(DC)}$.

7 Compare the test result against the compliance test limit.

$Slew_R$ Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ or DQS

Test Definition Notes from the Specification

Table 24 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Table 25 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Test References

See Table 21 - AC Input Test Conditions in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Rising Slew value of the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Pre-condition the oscilloscope setting.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use the Setup time and Hold time to find and capture the Write cycle.
4. Verify that V_{REF} and $V_{IH(AC)}$ points can be found on the oscilloscope screen.
5. Get the timestamp of V_{REF} and $V_{IH(AC)}$ threshold voltages.
6. Subtract the obtained timestamp values to calculate the delta TR.
7. Calculate the Rising Slew:

$$\mathrm{RisingSlew} = \frac{V_{IH(AC)}\mathrm{min} - V_{REF}}{\Delta TR}$$

8. When multiple trials are performed, the smallest value (worst case) among all the trials is used as the test result for $Slew_R$.
9. Compare test result with the compliance test limit.

$Slew_F$ Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQ or DQS

Test Definition Notes from the Specification

Table 26 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Table 27 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Test References

See Table 21 - AC Input Test Conditions, in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Falling Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Pre-condition the oscilloscope setting.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use the Setup time and Hold time to find and capture the Write cycle.
4. Verify that the V_{REF} and $V_{IL(AC)}$ points can be found on the oscilloscope screen.
5. Get the timestamp of V_{REF} and $V_{IL(AC)}$ threshold voltages.
6. Subtract the obtained timestamp values to calculate the delta TR.
7. Calculate the Falling Slew:

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(AC)}\text{max}}{\Delta TF}$$

8. When multiple trials are performed, the smallest value (worst case) among all the trials is used as the test result for $Slew_F$.
9. Compare test result with the compliance test limit.

5 Single-Ended Signals Overshoot/Undershoot Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR2 Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

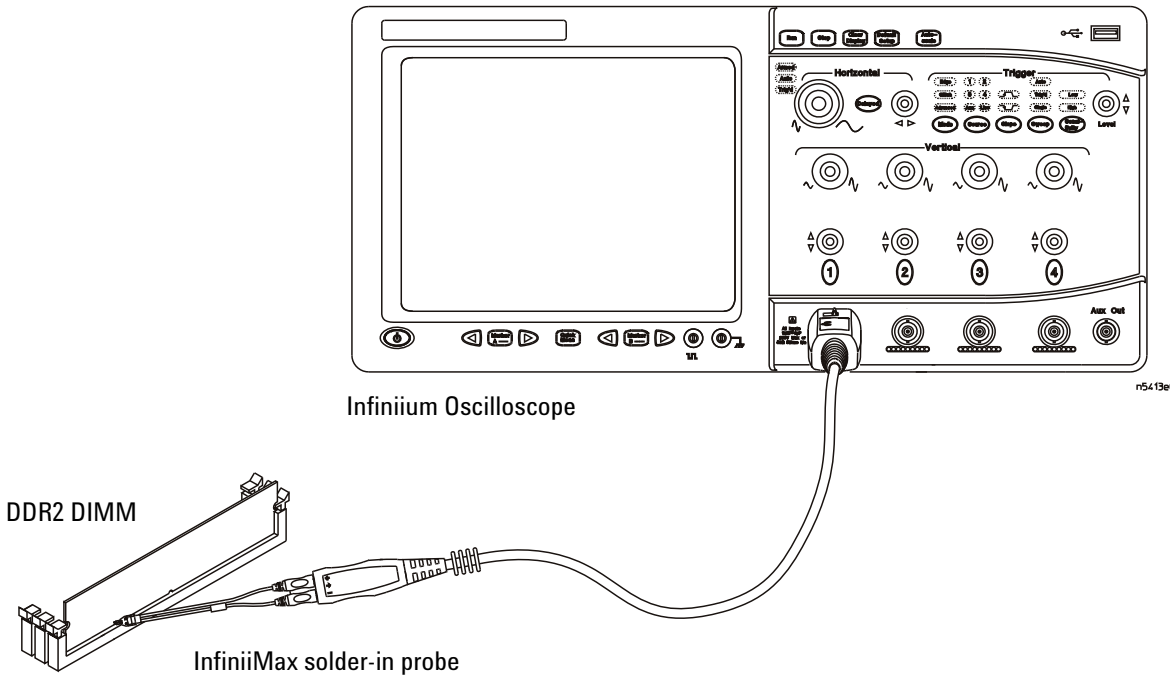

Figure 6 Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channel shown in Figure 6 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by

producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Single-Ended Signals Overshoot/Undershoot tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

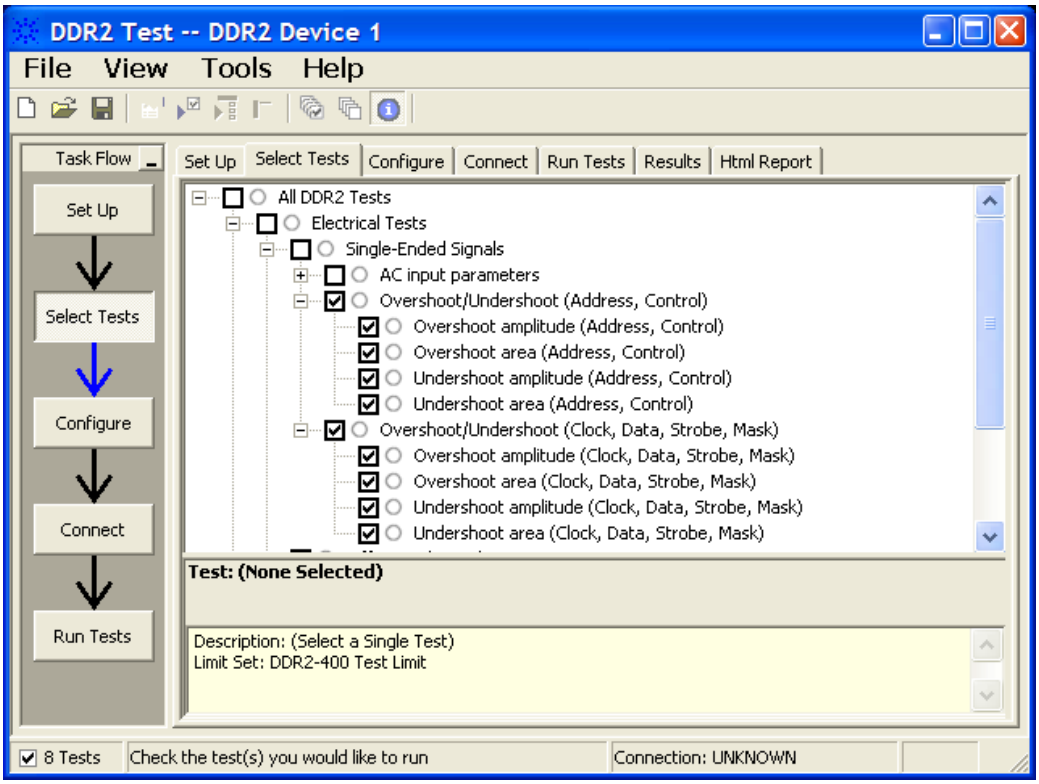

Figure 7 Selecting Single-Ended Signals Overshoot/Undershoot Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and overshoot area. The purpose of this test is to verify that the overshoot value of the test signal within a user-specific is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot test as specified in the JEDEC specification.

When there is an overshoot, the overshoot area is calculated based on the overshoot width. The overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 28 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum overshoot area above VDD	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

Table 29 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum overshoot area above VDDQ	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

Table 30 AC Overshoot/Undershoot Specification for Address and Control Pins (DDR2-1066)

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V
Maximum overshoot area above VDD	0.5 V-ns

Table 31 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins (DDR2-1066)

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for overshoot area	0.5 V
Maximum overshoot area above VDDQ	0.19 V-ns

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JEDEC Standard JESD79-2E*.

Also See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JESD208*.

PASS Condition

The measured maximum voltage value of the test signal should be less than or equal to the maximum overshoot value.

The calculated overshoot area value should be less than or equal to the maximum overshoot area allowed.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Initialize the oscilloscope settings.
4. Get the timestamp of the maximum peak voltage using all acquired waveforms at 10,000 Unit Interval (UI) length. Note: Unit Interval (UI) is the time length for one bit of data.
5. Get the timestamp of voltage value for VDD level closest to the peak point value in order to calculate the maximum overshoot length duration.
6. Calculate the overshoot area (V-ns)
   a. Area of calculation is based on the area of calculation of a triangle where the overshoot width is used as the triangle base and the overshoot amplitude is used as the triangle height.
   b. Area = 0.5 * base * height.
7. Compare the test results with the compliance test limits.

AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area. The purpose of this test is to verify that the undershoot value of the test signal within a region is lower than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot test as specified in the JEDEC specification.

When there is an undershoot, the undershoot area is calculated based on the undershoot width. The undershoot area should be lower than or equal to the conformance limit of the maximum undershoot area allowed as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ** or **WRITE**

Signal(s) of Interest:

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 32 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum undershoot area below VSS	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

Table 33 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum undershoot area below VSSQ	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

Table 34 AC Overshoot/Undershoot Specification for Address and Control Pins (DDR2-1066)

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V
Maximum undershoot area below VSS	0.5 V-ns

Table 35 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins (DDR2-1066)

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for undershoot area	0.5 V
Maximum undershoot area below VSSQ	0.19 V-ns

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-2E*.

Also See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JESD208*.

PASS Condition

The measured minimum voltage value for the test signal should be less than or equal to the maximum undershoot value.

The calculated undershoot area value should be less than or equal to the maximum undershoot area allowed.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Initialize the oscilloscope settings.
4. Get timestamp of the maximum peak voltage using all acquired waveforms at 10,000 Unit Interval (UI) length. Note: Unit Interval (UI) is the time length for one bit of data.
5. Get the timestamp of voltage value for VDD level closest to the peak point value in order to calculate the maximum overshoot length duration.
6. Calculate the undershoot area (V-ns)
   a. Area of calculation is based on the area of calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.
   b. Area = 0.5 * base * height.
7. Compare the test results with the compliance test limits.

6 Differential Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

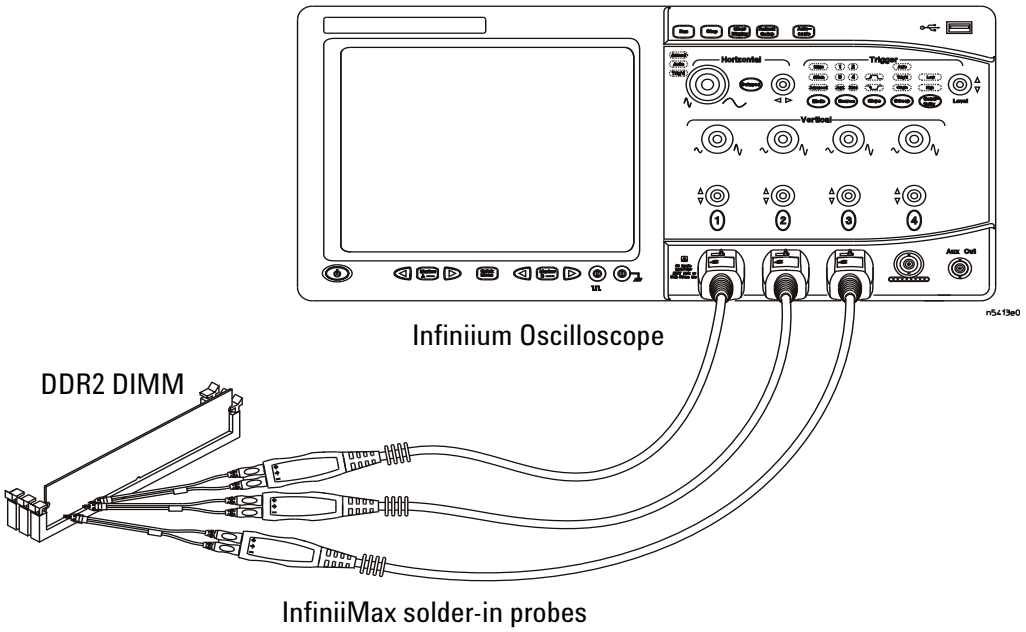

Figure 8 Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 8 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached.

This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

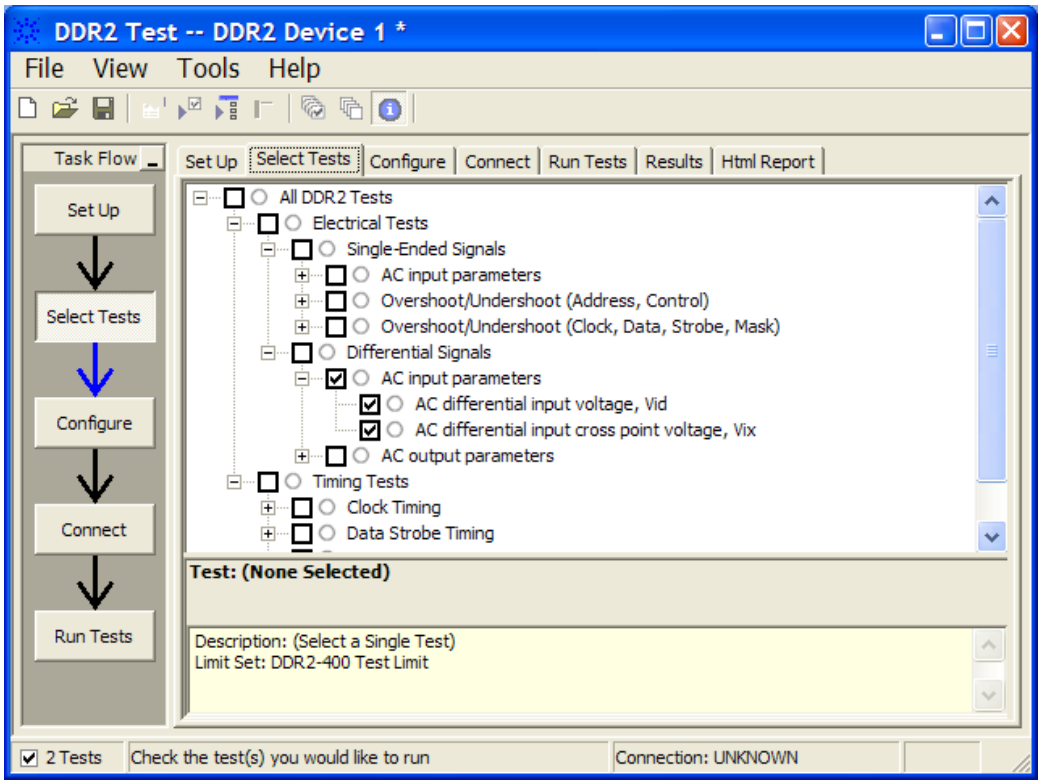

Figure 9 Selecting Differential Signals AC Input Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{ID(AC)}$, AC Differential Input Voltage - Test Method of Implementation

The purpose of this test is to verify that magnitude differences between the input differential signal pairs value of the test signals is within the conformance limits of the $V_{ID(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal) OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQS

Test Definition Notes from the Specification

Table 36 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	ac differential input voltage	0.5	V_{DDQ}	V	1,3

Table 37 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	ac differential input voltage	0.5	V_{DDQ} + 0.6	V	1

Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The calculated magnitude of the differential voltage of the test signals pair should be within the conformance limits of the $V_{ID(AC)}$ value.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Obtain sample or acquire data waveforms, for example CK+ and CK-.
4. Use histogram function (mode value) to find the nominal high level value for CK+ and nominal low level value for CK-.
5. Subtract the CK- low level value from the CK+ high level value.
6. Compare the test results with the compliance test limits.

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage -Test Method of Implementation

The purpose of this test is to verify the crossing point voltage value of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal) OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - only required when PUT is DQS.

Test Definition Notes from the Specification

Table 38 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	ac differential crosspoint voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

Table 39 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	ac differential crosspoint voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{IX(AC)}$ value.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Obtain sample or acquire data waveforms, for example CK+ and CK-.
4. Generate the differential waveform from two source input.
5. From the generated differential waveform, get the timestamp of voltage value = 0 V level (crossing point).
6. Get the actual crossing value using the obtained timestamp.
7. Compare the test results with the compliance test limits.

7 Differential Signal AC Output Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Output tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Differential Signals AC Output Parameters Tests

When performing Differential Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals AC Output Parameters tests may look similar to below diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

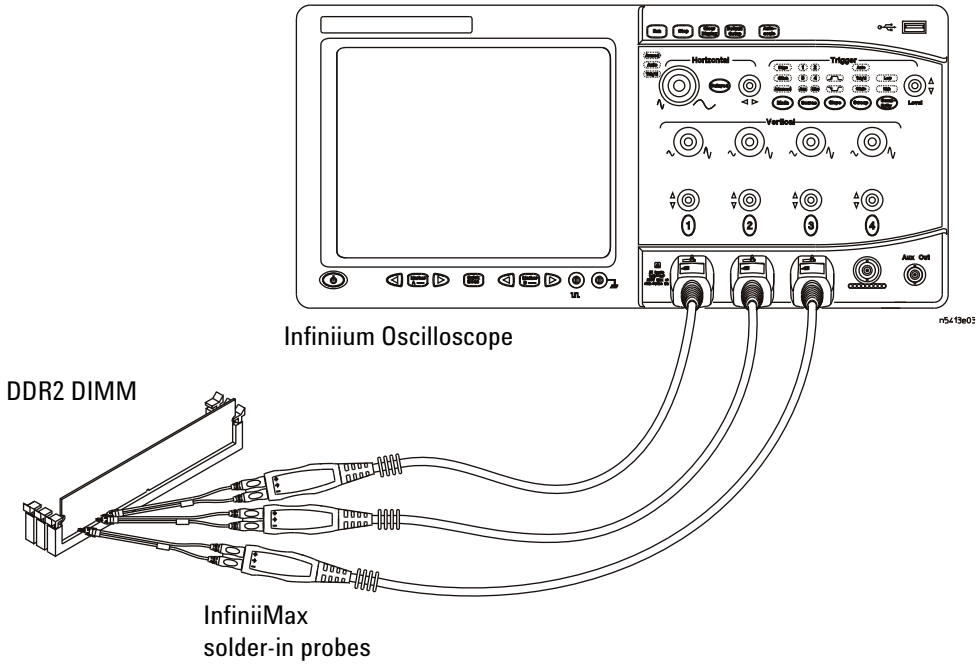

Figure 10 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 10 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system

by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals AC Output Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

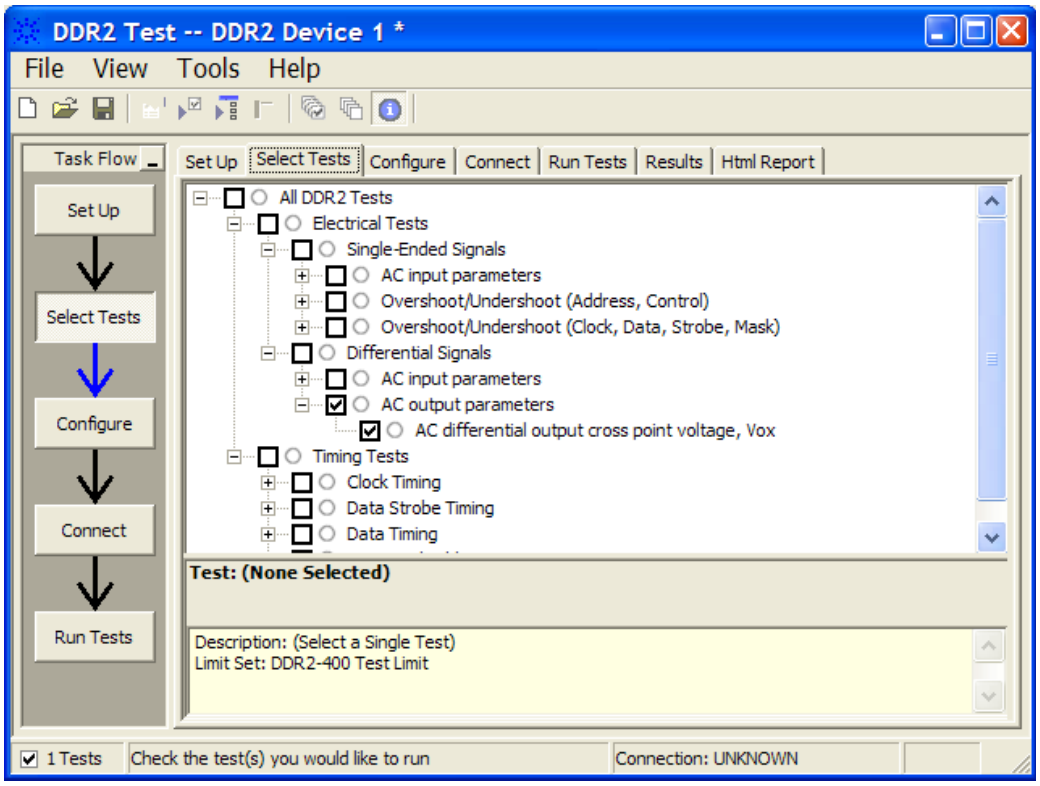

Figure 11 Selecting Differential Signals AC Output Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

V_{OX}, AC Differential Output Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point of the output differential test signals pair is within the conformance limits of the $V_{OX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - a corresponding DQ signal

Test Definition Notes from the Specification

Table 40 Differential AC Output Parameters

Symbol	Parameter	Min	Max	Units	Notes
$V_{OX(AC)}$	ac differential crosspoint voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Table 41 Differential AC Output Parameters (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{OX(AC)}$	ac differential crosspoint voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Test References

See Table 23 - Differential AC Output Logic Level in the *JEDEC Standard JESD79-2E* and Table 23 - Differential AC Output Logic Level in the *JESD208*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{OX(AC)}$ value.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Obtain sample or acquire data waveforms, for example CK+ and CK-.
4. Generate the differential waveform from two source input.
5. From the generated differential waveform, get the timestamp of voltage value = 0 V level (crossing point).
6. Get the actual crossing value using the obtained timestamp.
7. Compare the test results with the compliance test limits.

7 Differential Signal AC Output Parameters Tests

8 Clock Timing (CT) Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{XYZ}$ are referring to compliment. Thus, CK# is the same as $\overline{CK}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

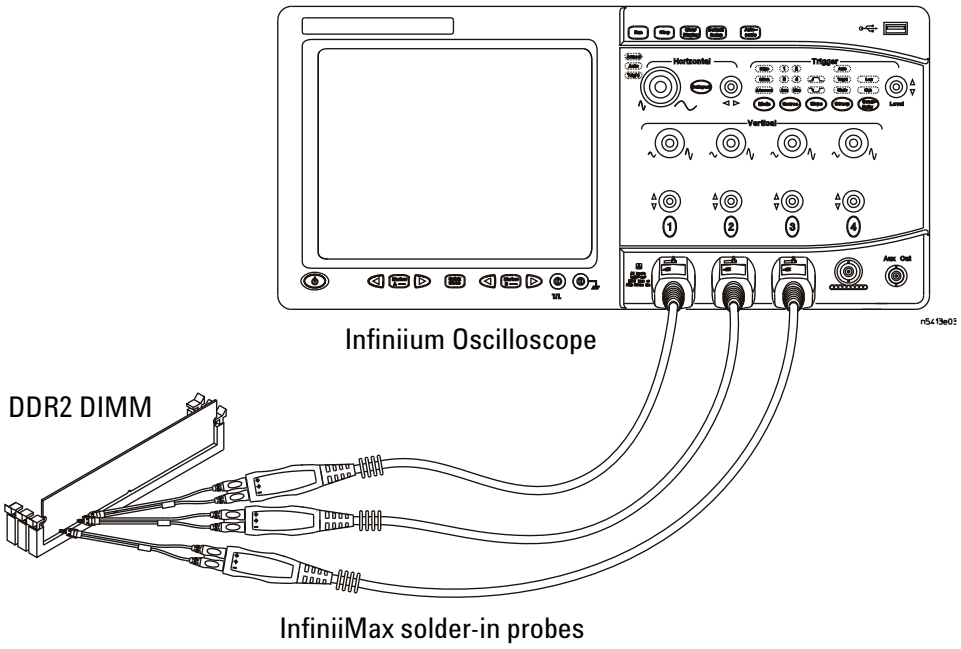

Figure 12 Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 12 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

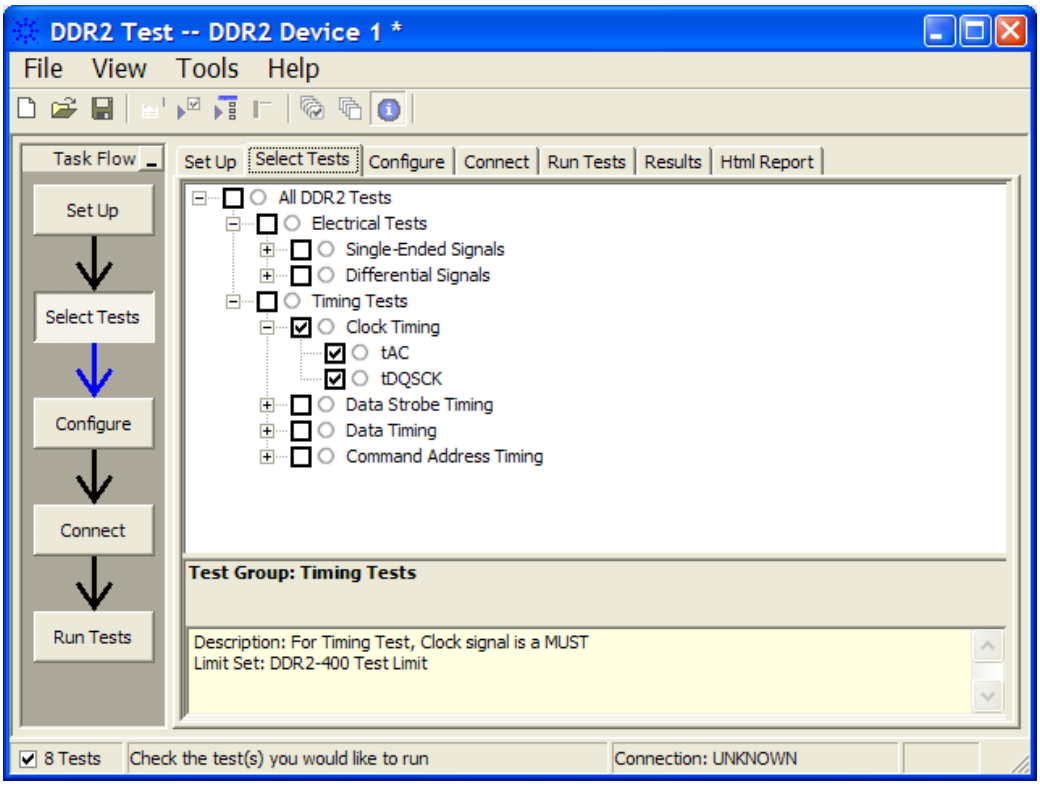

Figure 13 Selecting Clock Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

tAC, DQ Output Access Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time interval from data output (DQ rising and falling edge) access time to the nearest rising or falling edge of the clock must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 42 Timing Parameters by Speed Grade (DDR2-400 and DDR-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	450	-400	400	ps	40

Table 43 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-350	350	ps	35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data access output and rising edge of the clock should be within the specification limits.

Measurement Algorithm

1. Pre-condition the oscilloscope setting.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Begin the tAC measurement bit by bit in Read Data Burst. Begin at the 1st bit of the Read cycle, from the Read pre-amble. Continue the measurement until the last bit.

5 Within the data burst, each single bit is measured. Worst case data is captured each time a new value is measured.

6 Once all bits are validated, assign marker A for clock signal while marker B for data signal, for worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 44 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	400	-350	350	ps	40

Table 45 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-325	325	ps	35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data strobe access output and rising edge of the clock should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope setting.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Begin the tDQSCK measurement bit by bit in the Read data burst. Begin at the first bit of the Read cycle, from the Read preamble. Continue the measurement until last bit.

5 Within the data burst, measure each bit is measured. Worst case data is captured each time a new value is measured.

6 Once all bits are validated, assign marker A for clock signal while marker B for data signal, for worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

9 Data Strobe Timing (DST) Tests

This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

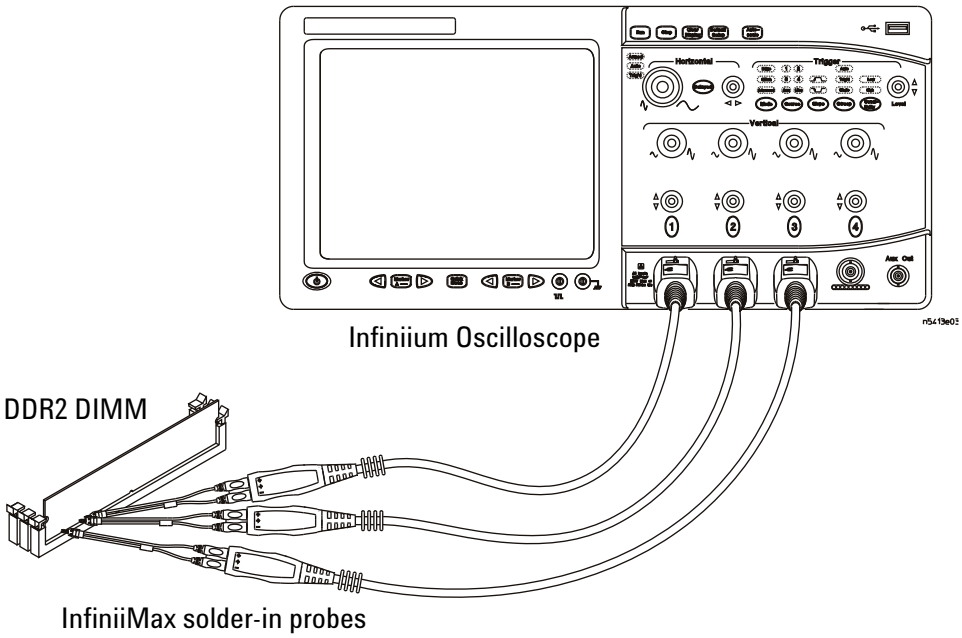

Figure 14 Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 14 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

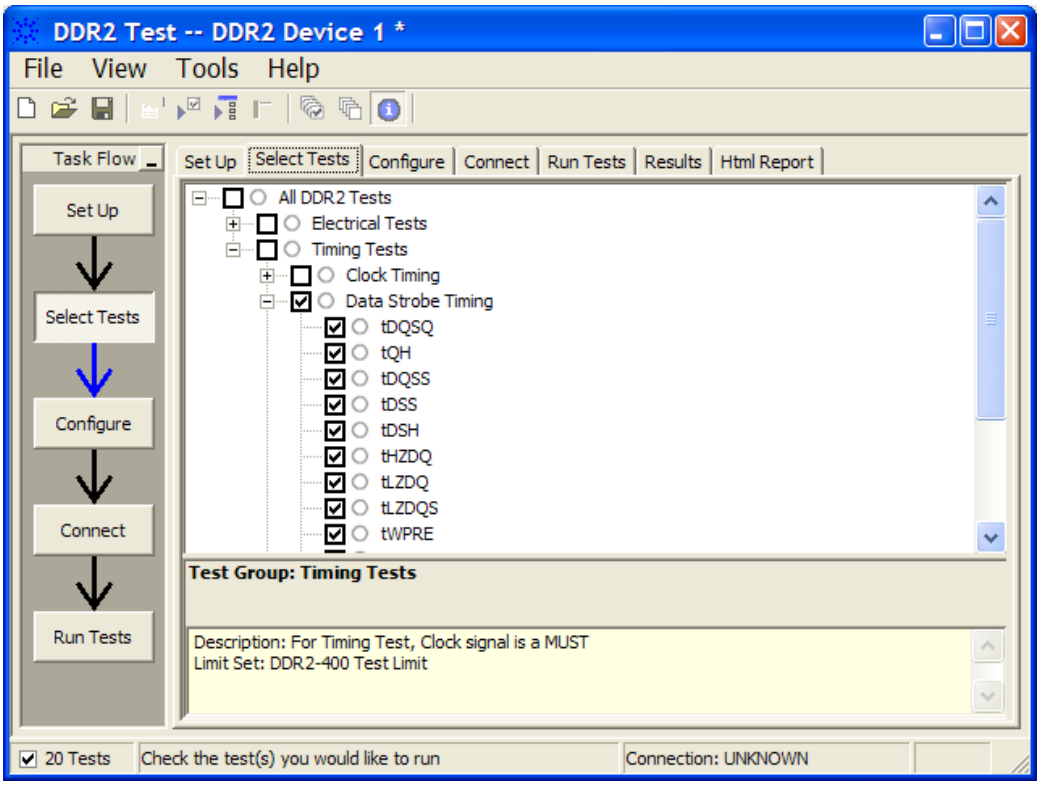

Figure 15 Selecting Data Strobe Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

tHZ(DQ), DQ Out HIGH Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from HIGH state OR LOW state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 46 Timing Parameter By Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18, 40

Table 47 Timing Parameter By Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	ps	15,35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from HIGH/LOW state to high impedance state, to the clock signal crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS postamble towards the right from the point where the Read cycle was previously captured.
4. Setup the threshold value and measurement point for the DQ signal.

5 Perform the trigonometry calculation to find the point where DQ starts transition from HIGH/LOW to the time when it turned off its driver into tri-state.

6 Assign marker A for the clock signal crossing point while marker B for the data signal start to turn off its driver.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

NOTE Some designs do not have tri-state at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tri-state to HIGH/LOW state) to the clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 48 Timing Parameter By Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18, 40

Table 49 Timing Parameter By Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	ps	15,35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval from the point where the DQS starts to transit from tri-state to the moment when it starts to drive HIGH/LOW (high impedance state to HIGH/LOW state) to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Setup the threshold value and measurement point for the DQS signal based on the histogram result.

5 Perform the trigonometry calculation to find the point where the DQS starts to transit from tri-state to the time when it start to drive HIGH/low.

6 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to HIGH/LOW state), to the clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 50 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18, 40

Table 51 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	ps	15,35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from high impedance to the moment when it starts to drive HIGH/LOW (high impedance state to HIGH/LOW state), to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Setup the threshold value and measurement point for the DQ signal based on the histogram result.

5 Perform the trigonometry calculation to find the point where the DQ starts to transit from tri-state to the time when it start to drive the signal HIGH/low.

6 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 52 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	240	-	200	ps	13

Table 53 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	175	ps	11

PASS Condition

The measured time interval between the data strobe and associated data signal should be within specification limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read Cycle was previously captured.
4. Begin the tDQSQ measurement bit by bit in the Read data burst, beginning from the 1st bit of the Read cycle.
5. Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit.

6 Within the data burst, each bit will be measured. Worst case data is captured each time a new value is measured.

7 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

8 Measure delta of marker A and marker B and this will be the test result.

9 Compare the test result against the compliance test limit.

tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQS rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 54 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	39

Table 55 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	ps	34

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data output hold time and associated data strobe signal should be within specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Begin the tQH measurement bit by bit in Read Data Burst, beginning from the 1st bit of the Read cycle.
5. Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit.

6 Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.

7 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

8 Measure delta of marker A and marker B and this will be the test result.

9 Compare the test result against the compliance test limit.

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 56 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK	

Parameter	Symbol	DDR2-667		DDR2-180		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	30

Table 57 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	tCK(avg)	25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the rising edge of the data strobe access output and the clock crossing should be within specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDQSS measurement bit by bit in the Write data burst, beginning from the 1st bit of the Write cycle. Begin at the 1st bit of the

Write cycle, from the Write preamble. Continue the measurement until the last bit.

5 Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.

6 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDQSH, DQS Input HIGH Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 58 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	

Table 59 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	tCK(avg)	

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured pulse width of the data strobe signal should be within specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDQSH measurement to find any rising edge of the data strobe signal and measure the pwidth for every single bit in the captured data burst.

5 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

6 Measure delta of marker A and marker B and this will be the test result.

7 Compare the test result against the compliance test limit.

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 60 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	

Table 61 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	tCK(avg)	

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured negative pulse width of the data strobe signal should be within specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDQSL measurement to find any rising edge of the data strobe signal and measure the nwidth for every single bit in the captured data burst.

5 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

6 Measure delta of marker A and marker B and this will be the test result.

7 Compare the test result against the compliance test limit.

tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 62 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30

Table 63 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	tCK(avg)	25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the falling edge of the data strobe access output to the associated clock setup time should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDSS measurement bit by bit in Write data burst.
5. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.

6 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 64 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30

Table 65 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	tCK(avg)	25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDSH measurement bit by bit in Write data burst. Begin at the first bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.

5 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

6 Measure delta of marker A and marker B and this will be the test result.

7 Compare the test result against the compliance test limit.

tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from HIGH/LOW state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 66 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10

Table 67 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
WRITE Postamble	tWPST	0.4	0.6	tCK(avg)	10

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from HIGH or LOW state to high impedance should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS postamble towards the right from the point where the Write cycle was previously captured.
4. Locate the last DQS crossing point or reference point.

5 Perform the trigonometry calculation to find the point where the DQS starts to transit from HIGH/LOW to the time when it starts to turn off the driver low.

6 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off driver.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tWPRE, Write Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts to drive LOW (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 68 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	

Table 69 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
WRITE Preamble	tWPRE	0.35	x	tCK(avg)	

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tri-state (high impedance state to low state) to the DQS signal crossing point for the Write cycle, should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Locate the first DQS crossing point or the reference point.
5. Perform the trigonometry calculation to find the point where the DQS starts to transit from tri-state to the time when it starts to drive low.

6 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving LOW (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 70 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19, 41

Table 71 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
READ Preamble	tRPRE	0.9	1.1	tCK(avg)	16,36

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tri-state (high impedance state to low state) to the DQS signal crossing point for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured.
4. Locate the first DQS crossing point or the reference point.
5. Perform the trigonometry calculation to find the point where the DQS starts to transit from tri-state to the time when it start to drive low.

6 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from HIGH/LOW state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 72 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19, 42

Table 73 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
READ Postamble	tRPST	0.4	0.6	tCK(avg)	16,37

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from HIGH/LOW level to high impedance for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope setting.
2. Use the Setup time and Hold time to find and capture the Read cycle.
3. Search for the DQS postamble towards the right from the point where the Read cycle was previously captured.
4. Locate the last DQS crossing point or reference point.

5 Perform the trigonometry calculation to find the point where the DQS starts to transit from HIGH/LOW to the time when it starts to turn off the driver low.

6 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off the driver.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

10 Data Timing Tests

This section provides the Methods of Implementation (MOIs) for Data Mask Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Timing Tests

When performing the Data Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Data Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

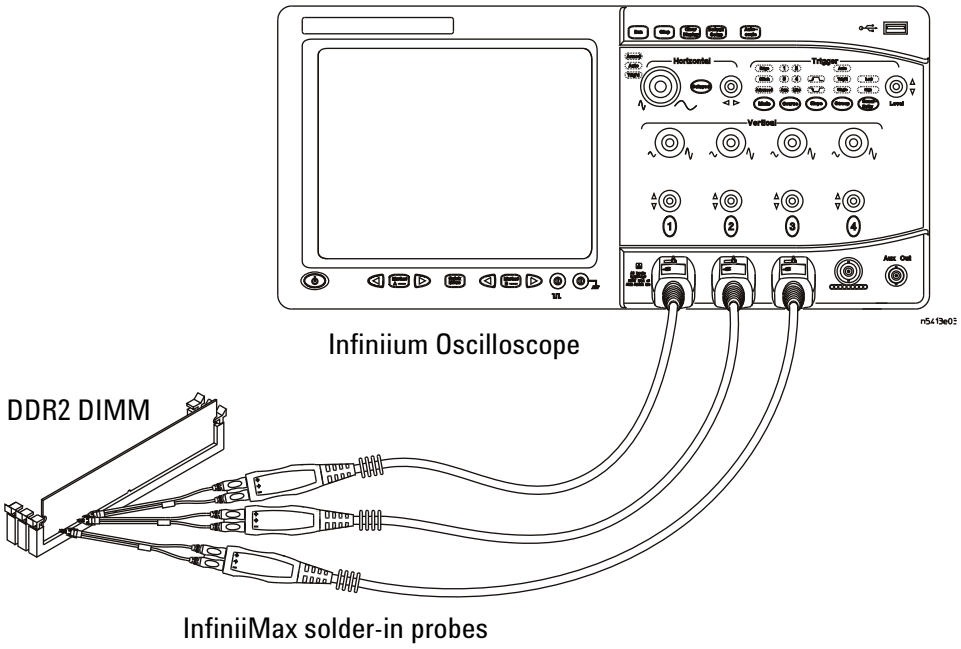

Figure 16 Probing for Data Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 16 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Data Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

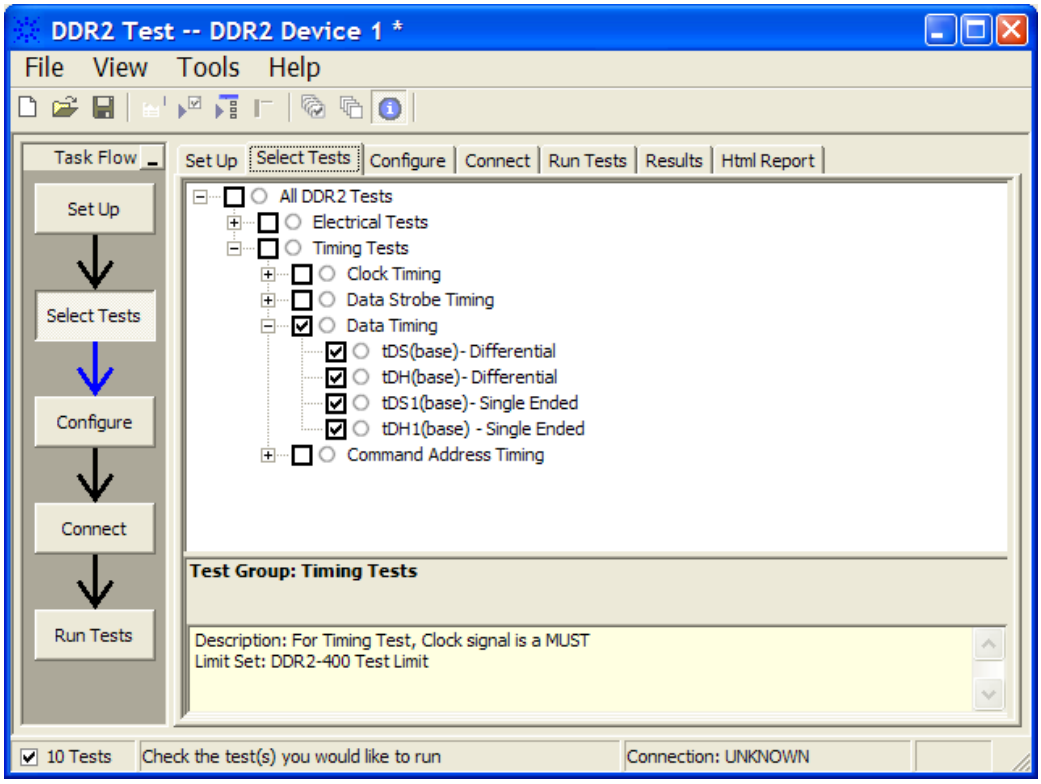

Figure 17 Selecting Data Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 74 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time	tDS(base)	100	x	50	x	ps	6,7,8,20,28,31

Table 75 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input setup time	tDS(base)	0	x	ps	6,7,8,17,23,26

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDS(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.

5 Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.

6 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 76 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	225	x	ps	6,7,8,21,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time	tDH(base)	175	x	125	x	ps	6,7,8,21,28,31

Table 77 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input hold time	tDH(base)	75	x	ps	6,7,8,18,23,26

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDH(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.

5 Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.

6 Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

7 Measure delta of marker A and marker B and this will be the test result.

8 Compare the test result against the compliance test limit.

tDS1(base), Single-Ended DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 78 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	-25	x	ps	6,7,8,25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2E*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS edge should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDS1(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.
5. Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.
6. Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

tDH1(base), Single-Ended DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 79 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	-25	x	ps	6,7,8,26

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2E*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS edge should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Use the Setup time and Hold time to find and capture the Write cycle.
3. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured.
4. Begin the tDH1(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit.
5. Within the data burst, each bit is measured. Worst case data is captured each time a new value is measured.
6. Assign marker A for the clock signal while marker B for the data signal, for the worst case bit.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

11 Command and Address Timing (CAT) Tests

This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Command Address Timing Tests

When performing the Command Address Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Command Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

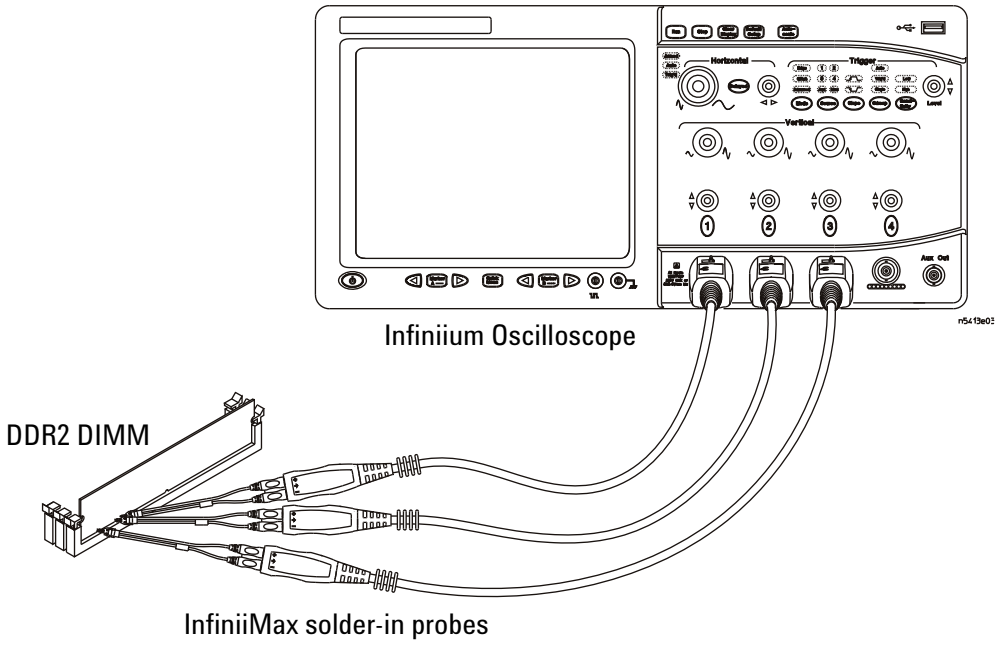

Figure 18 Probing for Command Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 18 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Command Address Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

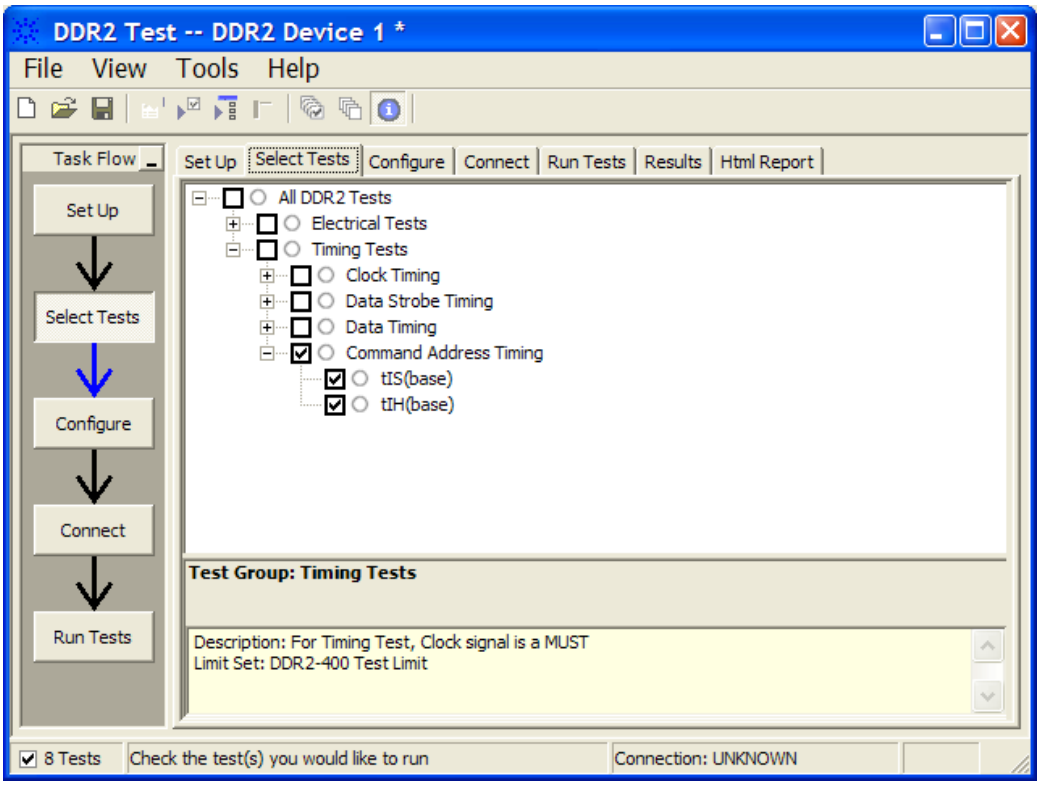

Figure 19 Selecting Command Address Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits of the $V_{ID(ac)}$ as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Address Signal OR Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 80 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	200	x	175	x	ps	5,7,9,22,29

Table 81 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input setup time	tIS(base)	125	x	ps	5,7,9,19, 24

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. tIS measurement compares the rising edge or falling edge setup time against the associated clock crossing edge.
3. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
4. Measure delta of marker A and marker B and the smallest delta value will be the test result.
5. Compare the test result against the compliance test limit.

tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Address Signal OR Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 82 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	275	x	250	x	ps	5,7,9,23,29

Table 83 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input hold time	tIH(base)	200	x	ps	5,7,9,20,24

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. tIH measurement compares the rising edge or falling edge hold time against the associated clock crossing edge.
3. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
4. Measure delta of marker A and marker B and the smallest delta value will be the test result.
5. Compare the test result against the compliance test limit.

12 Custom Mode Read-Write Eye-Diagram Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode Read-Write Eye-Diagram tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Custom Mode Read-Write Eye Diagram Tests

When performing the Custom Mode Read-Write Eye Diagram tests, the DDR2 Compliance Test Application will prompt you to make the proper connections as shown in Figure 20.

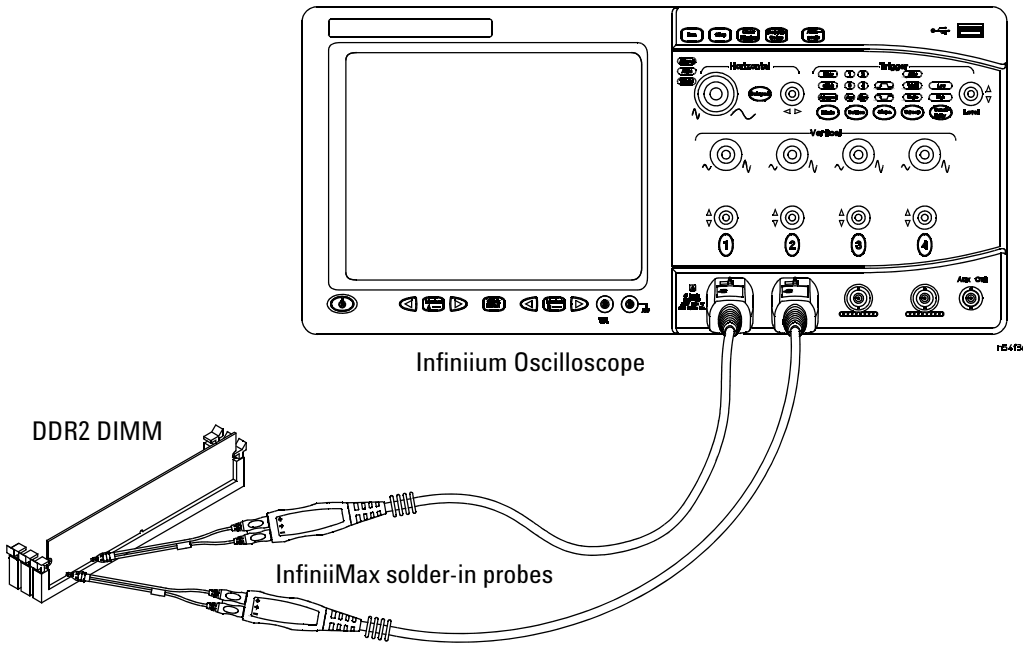

Figure 20 Probing for Custom Mode Read-Write Eye Diagram Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 20 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 193.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing repetitive bursts of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR2 Test application, click the Set Up tab.

6 Select Custom as the Test Mode option. This selection shows an additional command button - **Set Mask File**.

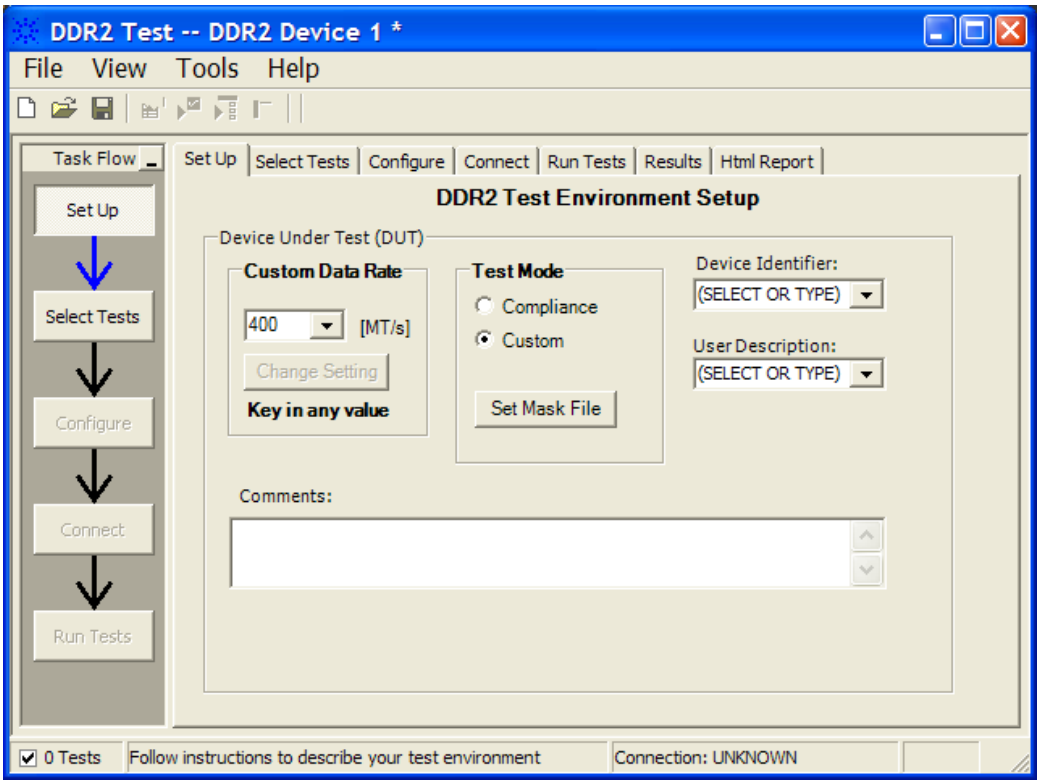

Figure 21 Selecting Custom Test Mode

7 Click this button to view or select test mask files for eye diagram tests.

Figure 22 Selecting Test Mask for Eye Diagram Tests

8 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

9 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

10 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

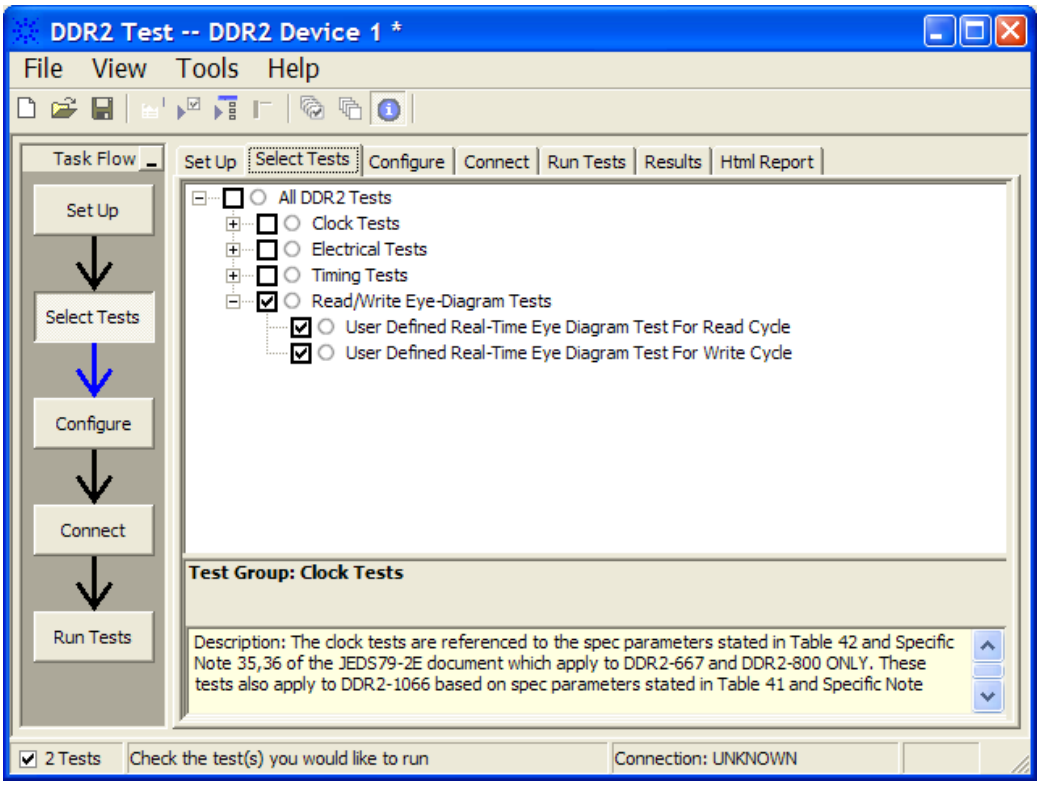

Figure 23 Selecting Advanced Debug Read-Write Eye-Diagram Tests

11 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Advanced Debug Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Signal cycle of interest: **READ**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - DQ Signal
- Supporting Pin - DQS Signal

Measurement Algorithm

1. Use the Setup time and Hold time to find and capture the Read cycle.
2. Setup the oscilloscope to generate eye diagram.
3. Start the mask test.
4. Loop until the number of required waveforms is acquired.
5. Obtain and display the total failed waveforms as the test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the JEDEC specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Signal cycle of interest: **WRITE**

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - DQ Signal
- Supporting Pin - DQS Signal

Measurement Algorithm

1. Use the Setup time and Hold time to find and capture the Write cycle.
2. Setup the oscilloscope to generate eye diagram.
3. Start the mask test.
4. Loop until the number of required waveforms is acquired.
5. Return the total failed waveforms as the test result.

13 Calibrating the Infiniium Oscilloscope and Probe

This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR2 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 80000B and 90000A series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap.

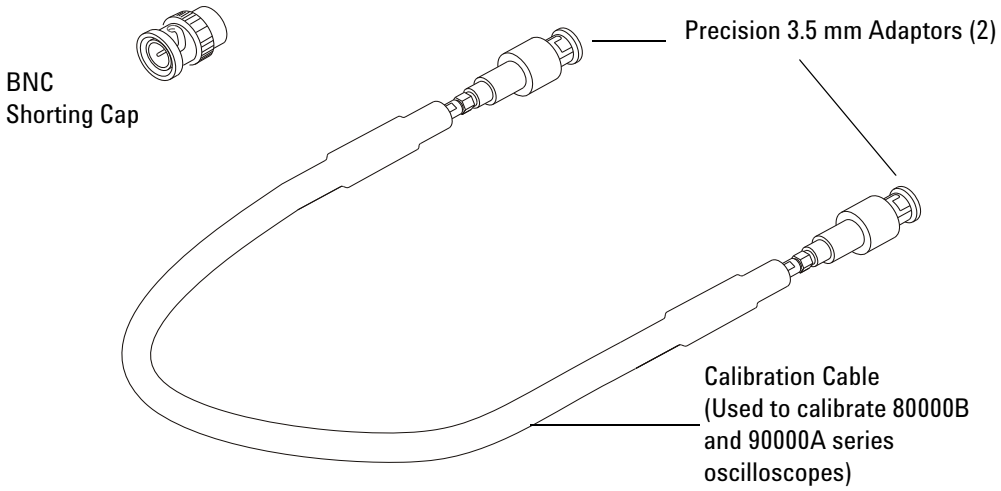

Figure 24 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

- **a** Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
- **b** Plug in the power cord.
- **c** Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
- **d** Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 25 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

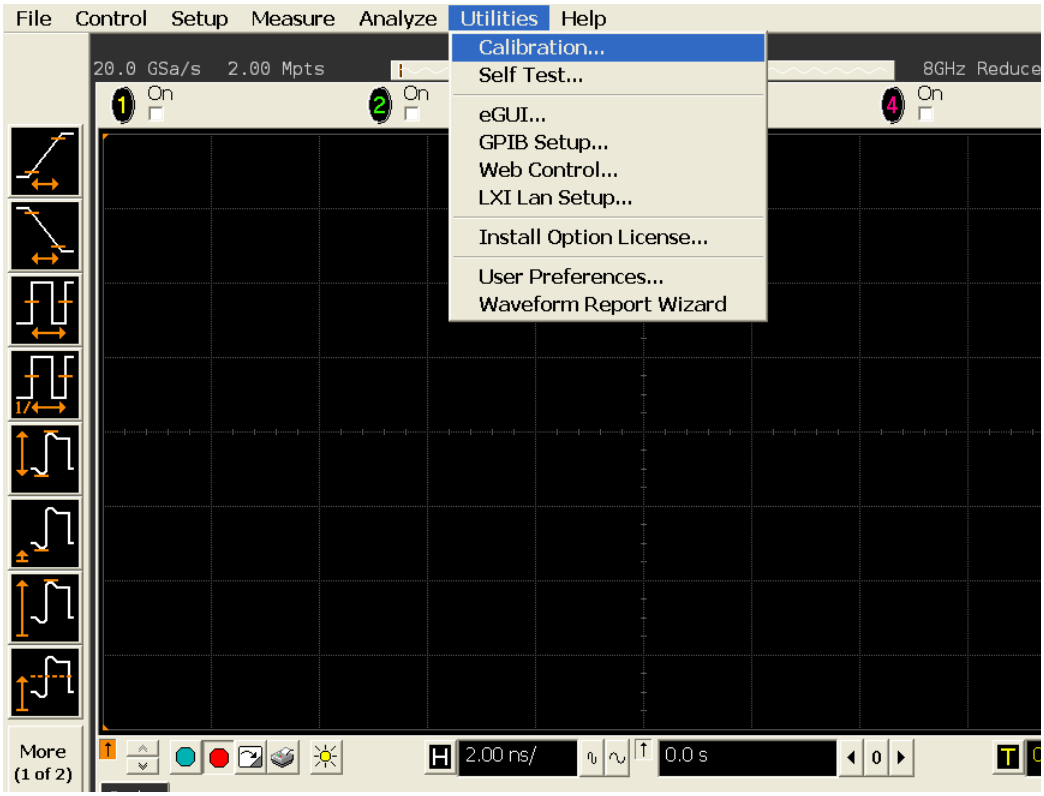

Figure 25 Accessing the Calibration Menu

4 Referring to Figure 26 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

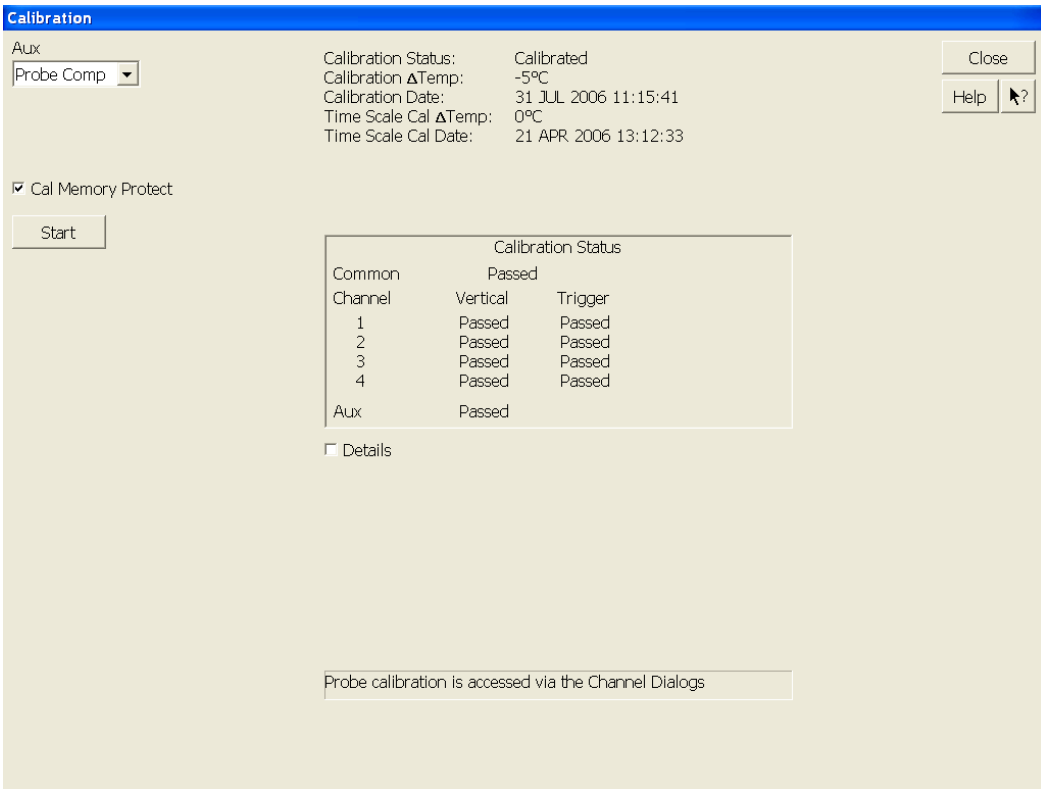

Figure 26 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 27 below.

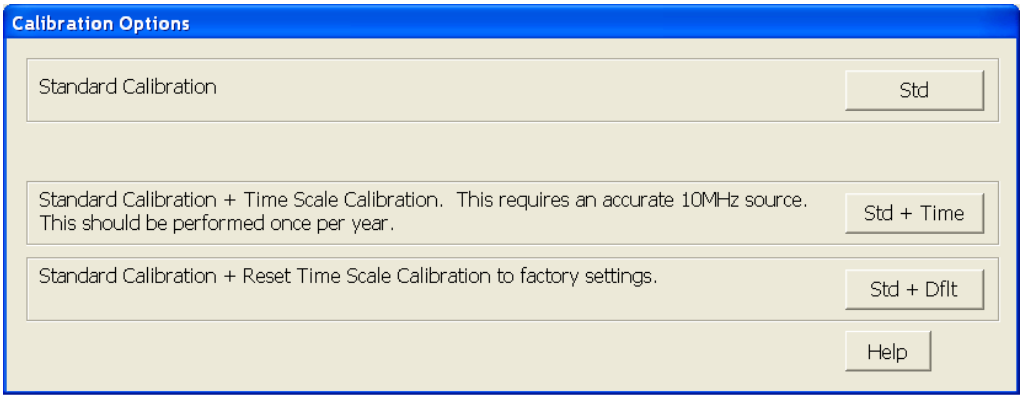

Figure 27 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing DDR2 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 28 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

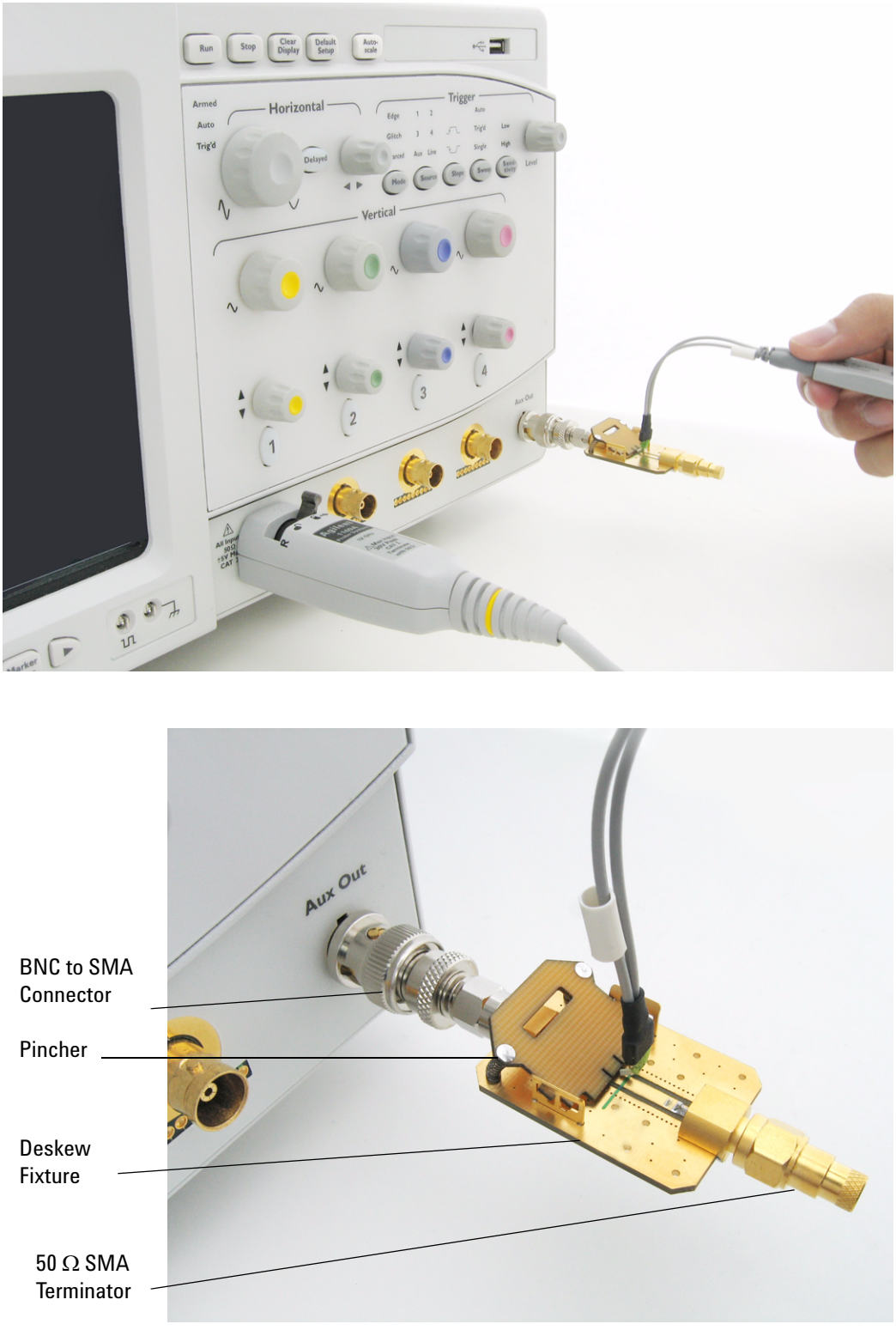

Figure 28 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 29 below.

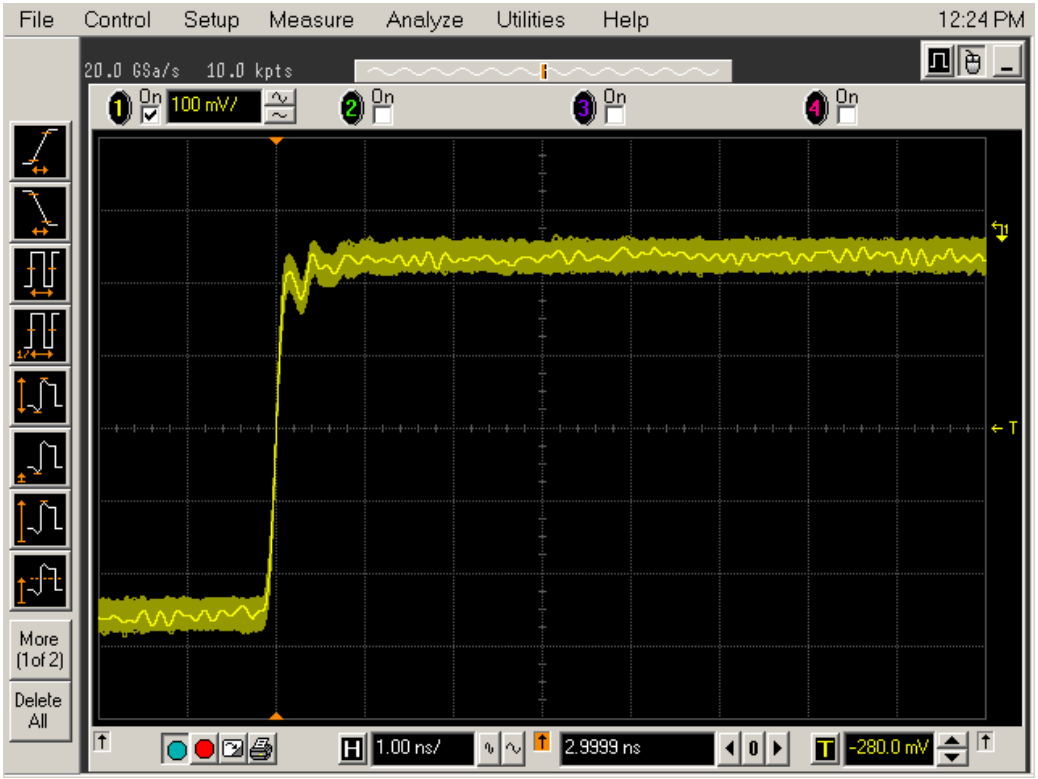

Figure 29 Good Connection Waveform Example

If you see a waveform similar to that of Figure 30 below, then you have a bad connection and should check all of your probe connections.

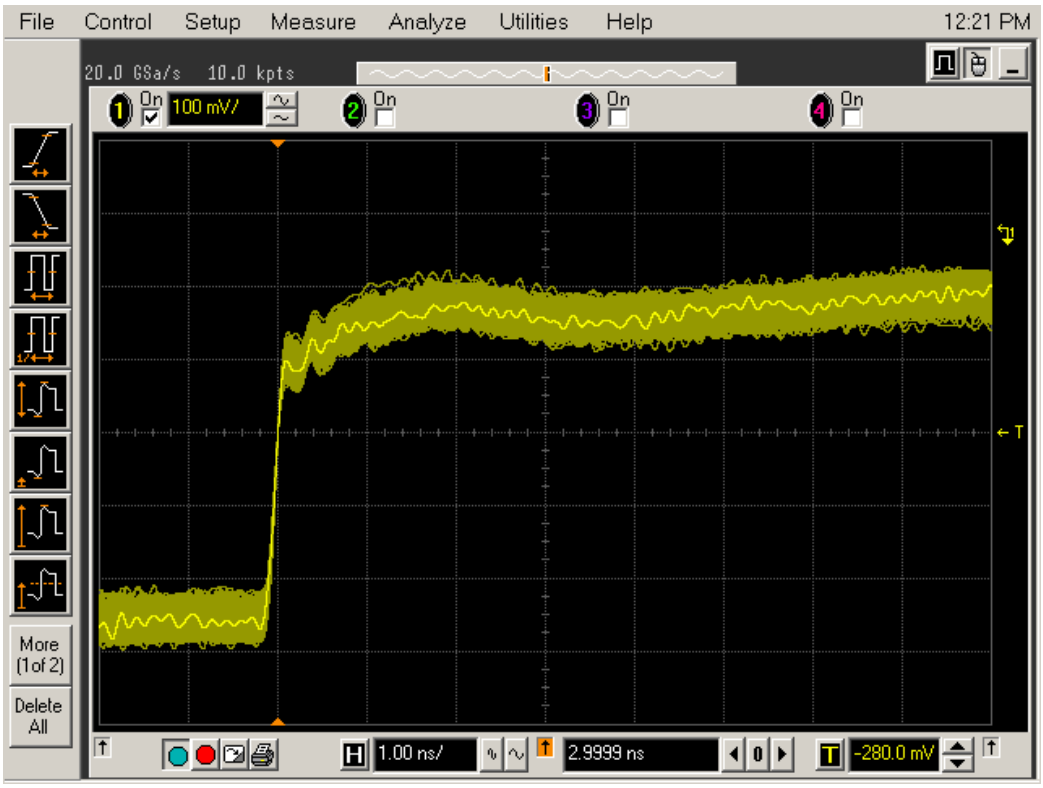

Figure 30 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 31.

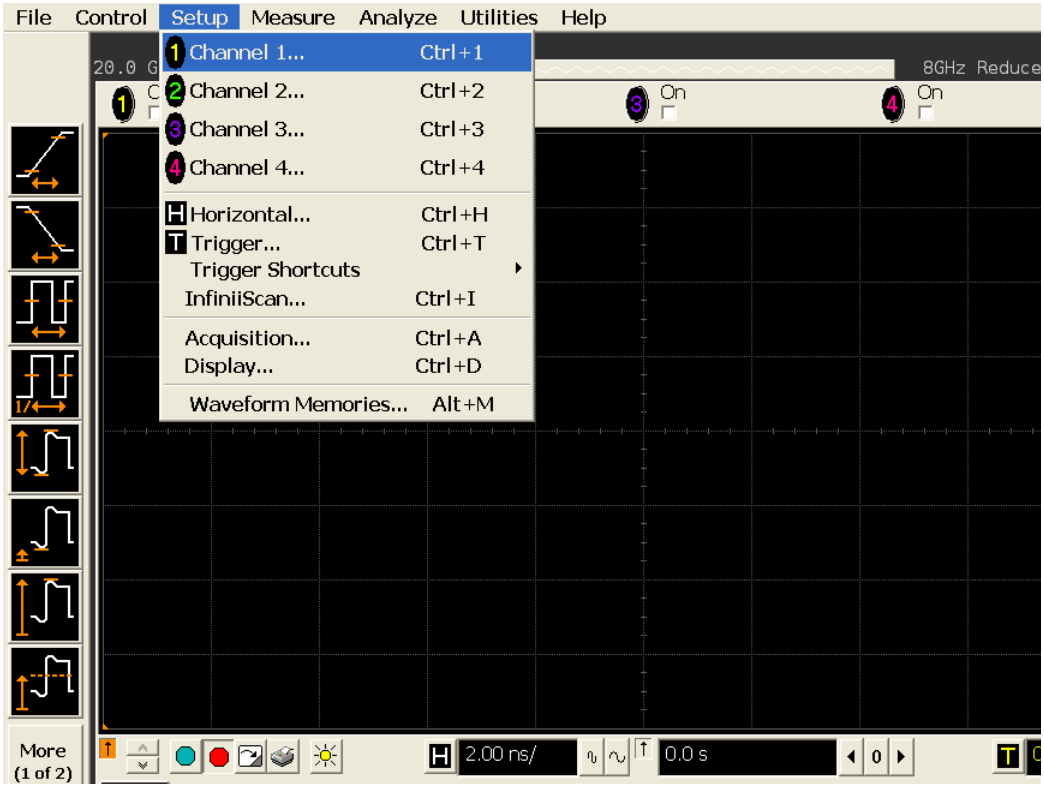

Figure 31 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 32.

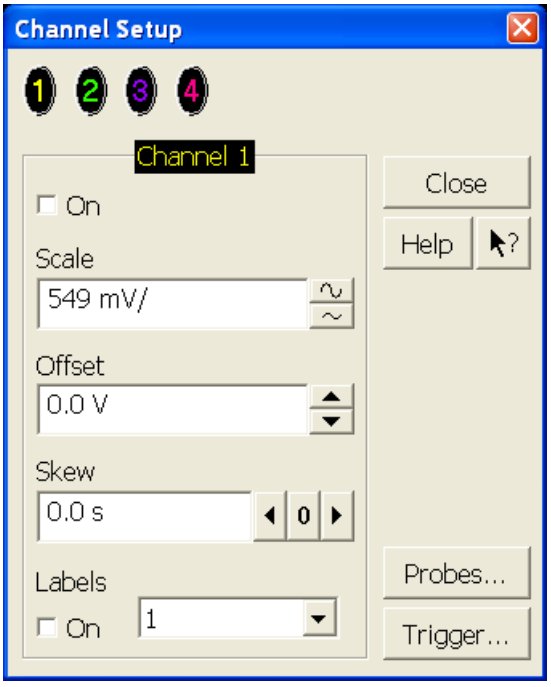

Figure 32 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

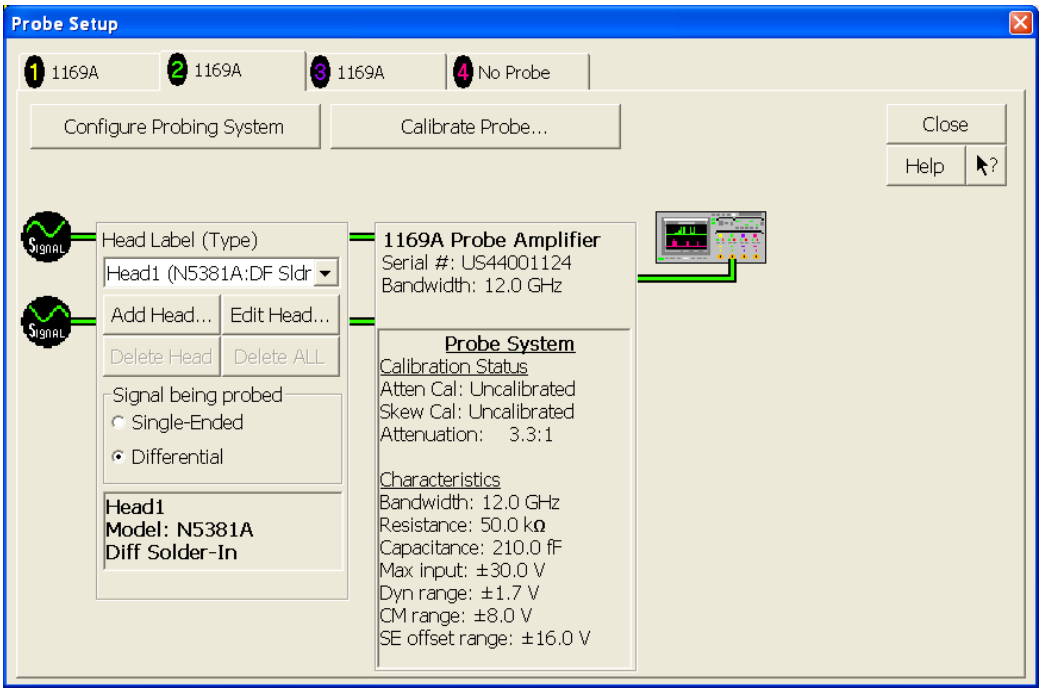

Figure 33 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

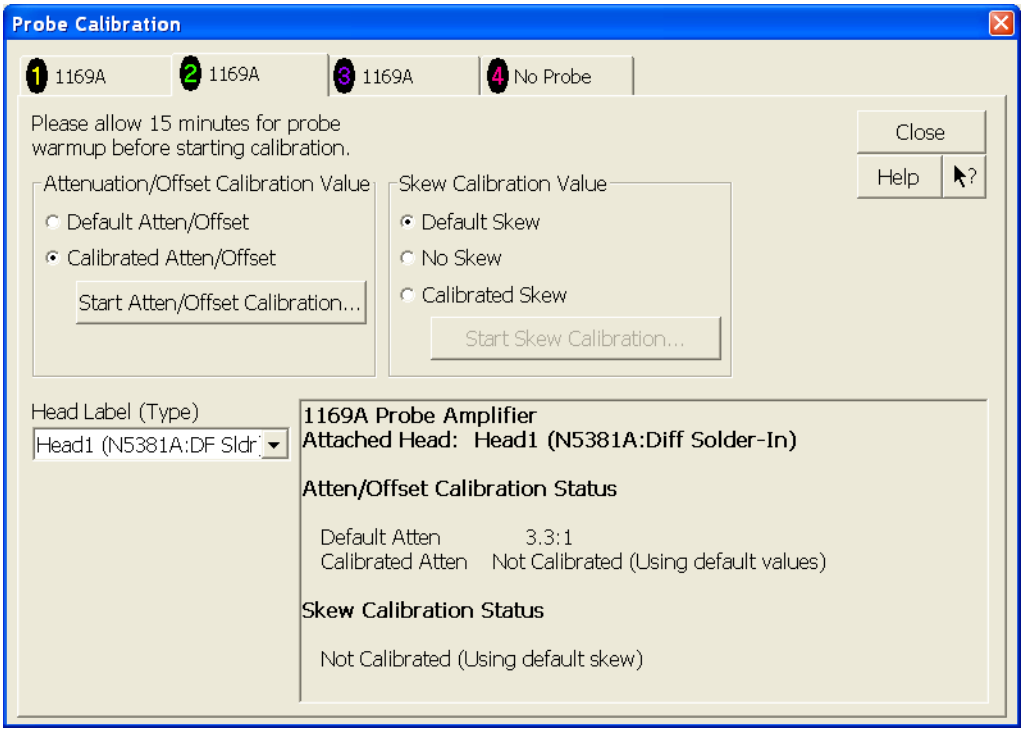

Figure 34 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838
- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 35.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

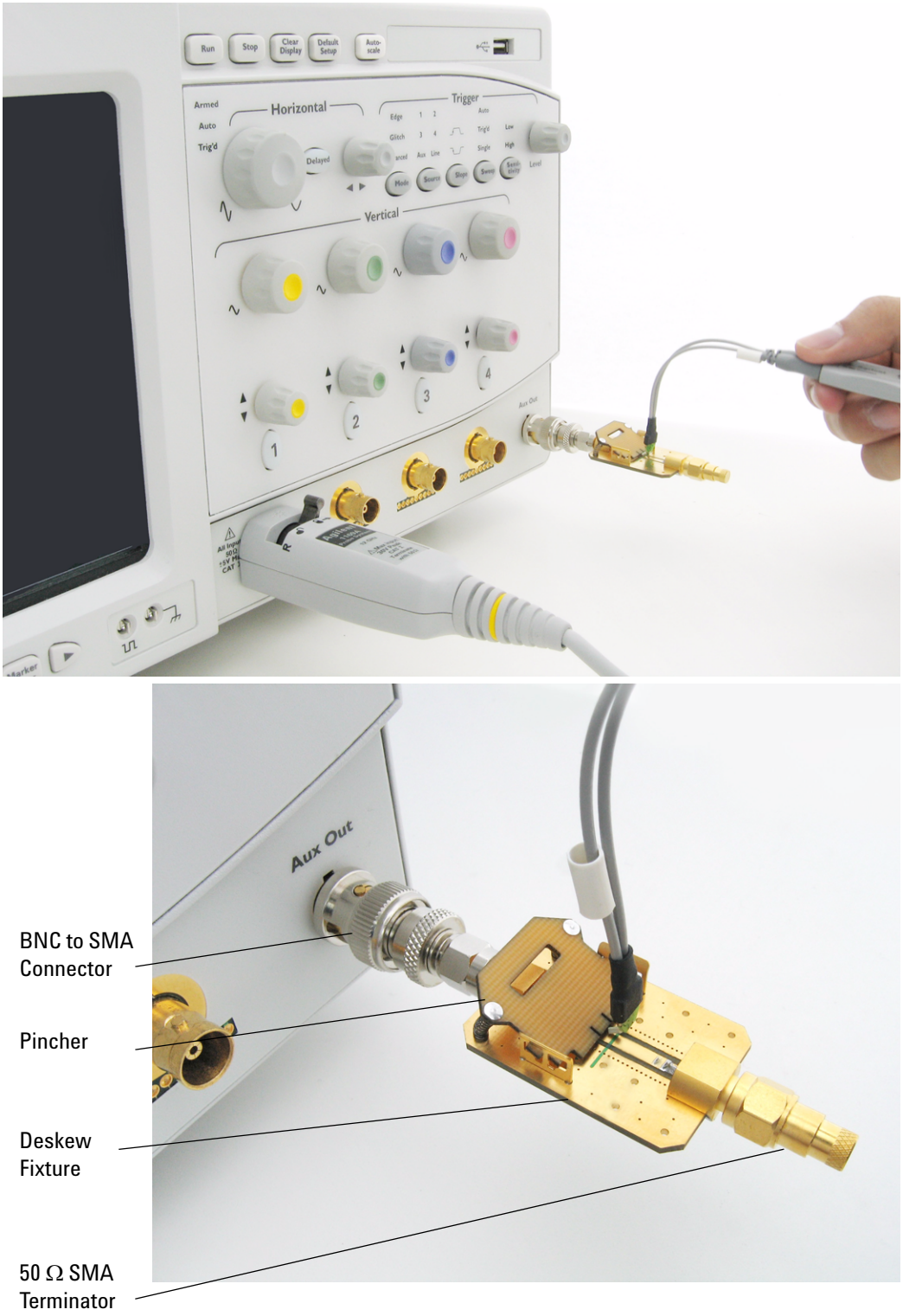

Figure 35 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 36.

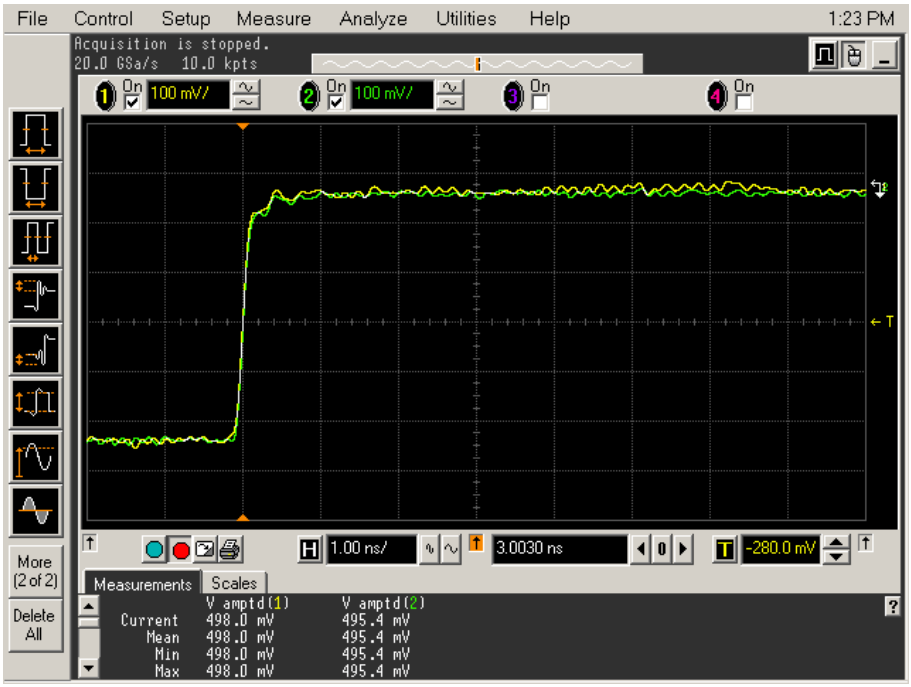

Figure 36 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

14 InfiniiMax Probing

Figure 37 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 38 E2677A / N5381A Differential Solder-in Probe Head

Table 84 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

Index

U

V

W

Z

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Sixth edition, November 2009
This part is not orderable.

N5413-97005

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